

Ultra Low Ron SiC Trench Devices

Keiji OKUMURA, Nobuhiro HASE, Kazuhide INO,

Takashi NAKAMURA, and Masanori TANIMURA

ROHM Co., Ltd.

21 Saiin Mizosaki-cho, Ukyo-ku, Kyoto, 615-8585, Japan

Email: sic@rohm.co.jp

Abstract

This paper presents next generation Silicon Carbide (SiC) planar MOSFETs, trench structure Schottky diodes, and trench MOSFETs. Firstly, developed SiC planar MOSFETs have suppressed the degradation of parasitic PN junction diodes even if forward current penetrates into the PN junction diodes. Secondly, SiC Schottky diodes, with newly developed trench structures, successfully showed lower forward voltage than conventional SiC diodes while keeping leakage current at an acceptable level. Thirdly, developed SiC MOSFETs with a double-trench structure have improved reliability of the device while maintaining ultra low on-resistance due to the fact that the new structure effectively reduced the highest electric field at the bottom of the gate trench, preventing gate oxide breakdown.

1. Newly Developed SiC devices

1.1. Developed SiC Planar MOSFETs

Some companies have already begun mass production of SiC planar MOSFETs for the sake of lower switching losses in high voltage applications such as converters and inverters. However, on-resistance increases when current flows into the parasitic body diodes of these mass-produced MOSFETs. This is because the parasitic PN body diodes, with the base plane dislocation, induce expansion of stacking faults in 4H-SiC epilayers and degrade the on-resistance of both the body diodes and MOSFETs. This is an obstacle for application in circuits which require current penetration from source to drain such as converters and inverters at the mass production level. However, some groups have reported no degradation of PN diodes at the research level.

Our group developed substrate, epitaxy and device fabrication processes to prevent degradation of the body diodes. Fig.1 and Fig.2 show MOSFETs on-resistance evaluation and differential on-resistance of the body diodes after continuous current penetration, respectively. We compared 2 conventional planar MOSFETs with 22 developed planar MOSFETs. Blocking voltage of the MOSFETs evaluated is 1200 V. On resistance is typically 0.09 Ω . Die size and active area are 13.2 mm² and 10 mm², respectively. Applied continuous current from source to drain of the MOSFET is 8 amperes.

After 24 hours continuous current application, conventional planar MOSFETs have drastically increased both on-resistance of MOSFETs and differential on-resistance of body diodes. On the other hand, developed planar MOSFETs have suppressed the degradation of on-resistance even after 1000 hours current application.

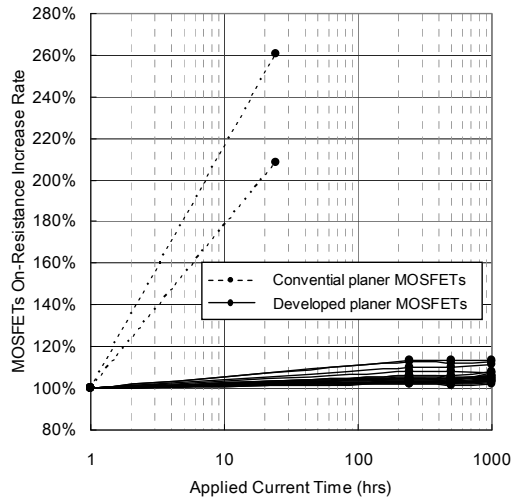


Fig. 1. Comparison of MOSFETs on-resistance increase rate after current application

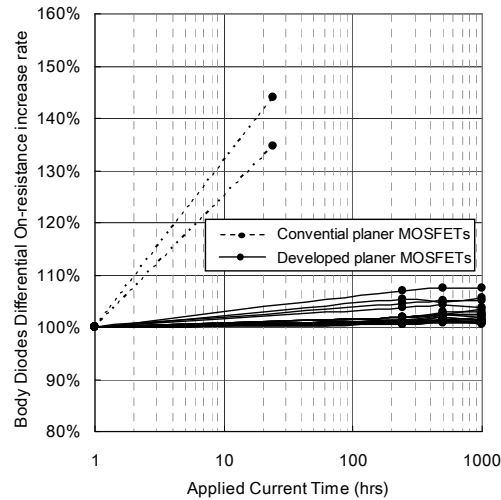
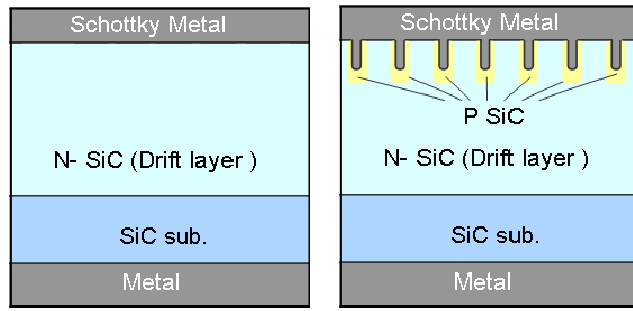


Fig. 2. Comparison of body diodes differential on-resistance increase rate after current application

1.2. SiC Trench Structure Schottky Diodes

SiC Schottky diodes are attractive devices to reduce switching losses in high voltage applications. The reduction of conductive losses is also required to improve efficiency. However, SiC Schottky diodes have higher forward voltage drop when compared to silicon PN junction diodes. The reason is that SiC Schottky diodes need high barrier heights to block leakage current because SiC has a breakdown strength 10 times greater than that of silicon. The reduction of electric fields at the Schottky interface is crucial for SiC Schottky diodes.

Our group have proposed the trench structure Schottky diodes to obtain a lower forward voltage drop while maintaining the same leakage current [1]. Fig.3 shows the schematic cross section of a 4H-SiC planar and trench structure Schottky diode. Trench p region can suppress the concentration of electric field at the Schottky interface. Fig.4 shows reverse bias simulation results of the electric field distribution. Fig.5 indicated the highest electric field at the Schottky interface of the planar structure and the trench structure is 1.65 MV/cm and 0.68 MV/cm, respectively. The simulation shows a lower barrier height can be obtained by using a trench structure.



(a) the planar structure (b) the trench structure

Fig. 3. Schematic cross section of the planar and trench structure Schottky diodes.

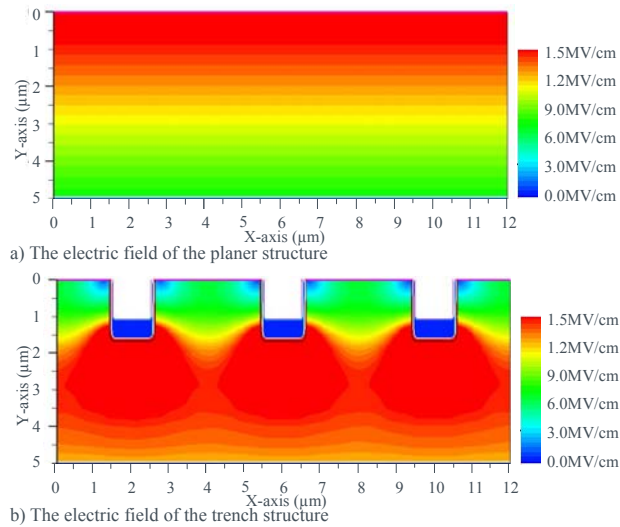


Fig. 4. Reverse bias simulation results at 600 V.

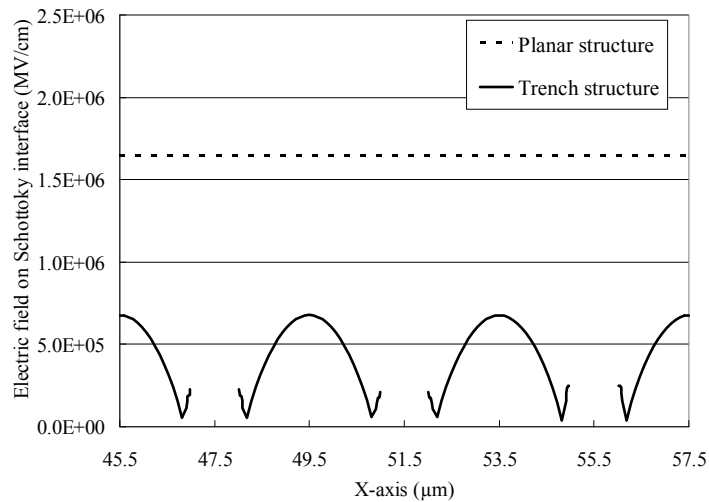


Fig. 5. Electric field at the Schottky interface of the planar structure and the trench structure

Schottky diodes with the planar structure and trench structure were fabricated. The barrier heights of the planar structure and the trench structure are different at 1.31 eV and 0.85 eV, respectively. Trenches are 1.05 μm deep. The diode die size is 3.06 mm^2 . Fig.6 shows the

forward IV characteristics of fabricated diodes which were assembled into TO-220 packages. The threshold voltage of the trench structure is 0.48 V smaller than that of the planar structure. The smaller threshold voltage can reduce the conductive losses during forward current operation. Fig.7 shows the reverse IV characteristics. The leakage current at 600 V is the same level in both devices.

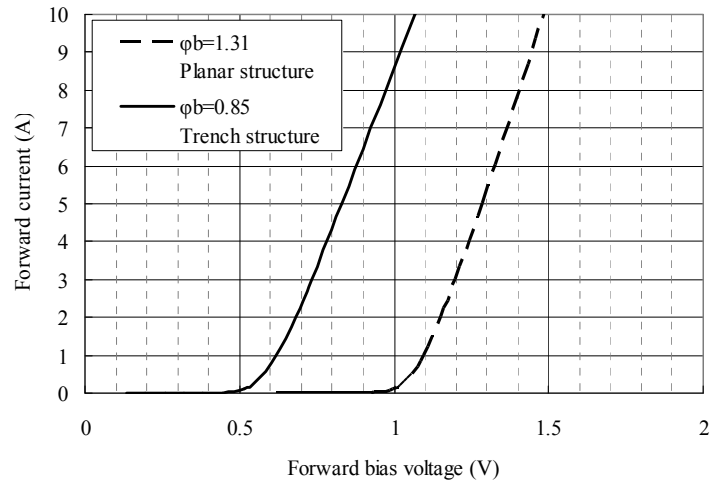


Fig. 6. The forward IV characteristics of the planar and trench Schottky diodes

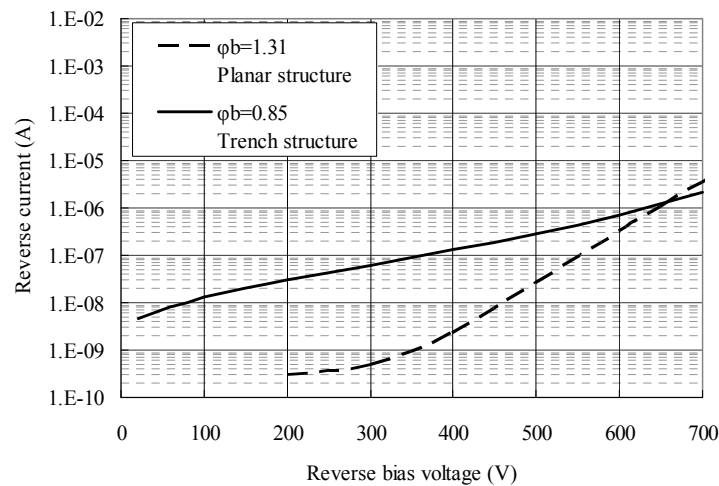


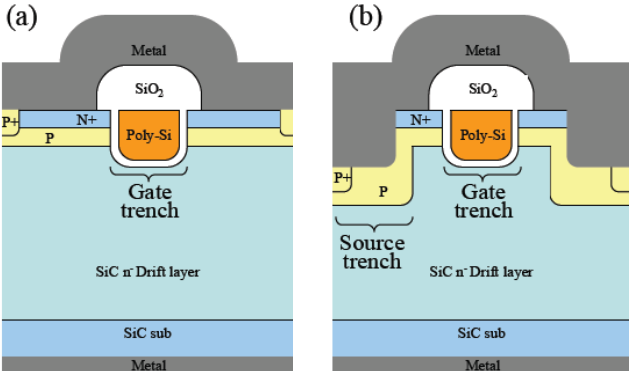
Fig. 7. The reverse IV characteristics of the planar and trench Schottky diodes.

1.3. SiC Double-Trench MOSFETs

SiC trench MOSFETs can have lower conductive losses when compared with planar MOSFETs because planar MOSFETs have JFET regions which increase the on-resistance [2][3]. Our group previously reported 790 V SiC trench MOSFETs with the lowest Ron at room temperature. However, the trench MOSFETs had issues regarding oxide breakdown at the trench bottom during high drain-source voltage application. To resolve issue of gate oxide breakdown, double-trench MOSFET structure, which has both source and gate trenches, was developed [4][5].

The device structures for the single and double-trench structures are shown in Fig.8(a) and (b), respectively. To suppress electric field at the gate oxide bottom, the source trench is fabricated deeper than gate trench. Fig.9 and Fig.10 show drain-source bias simulation results of the electric field distribution at 600 V with a gate-source voltage of 0 V. In the single-trench structure the highest electric field at the bottom of the gate trench was 2.66 MV/cm. On the

other hand, that figure was effectively reduced to 1.66 MV/cm in the double-trench structure. Deeper source trenches prevent the concentration of electric fields at the bottom of the gate trench.



(a) the single-trench structure (b) the double-trench structure

Fig. 8. Schematic cross section of 4H-SiC trench MOSFET with source trench and gate trench

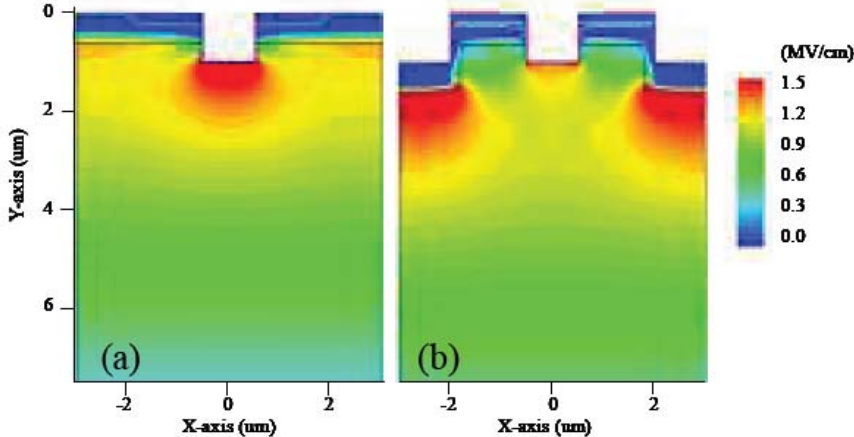


Fig. 9. Drain-source bias simulation results at 600 V with a gate-source voltage 0V

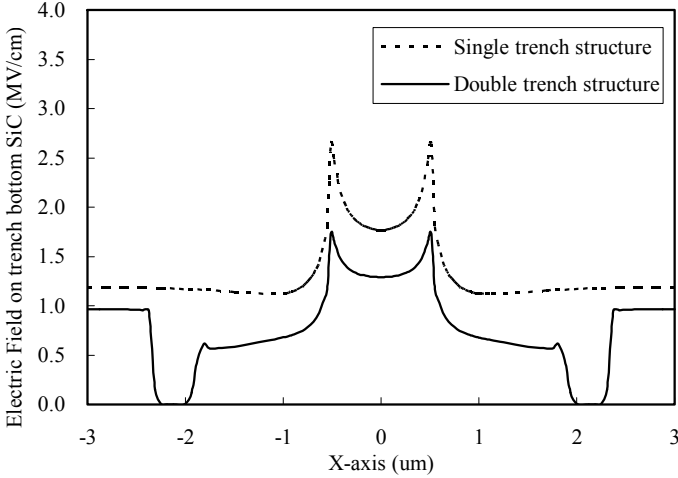


Fig. 10. Electric field for the single trench structure and the double-trench structure

Double-trench MOSFETs are fabricated using 2 different epilayers. The trench depth was typically 1.0 μm . The thickness of gate oxide was about 50 nm.

The measured channel mobility on the trench sidewalls of the fabricated double-trench MOSFETs was about $11\text{cm}^2/\text{Vs}$. The charge to oxide breakdown estimated by CCS-TDDB (constant current stress time dependence dielectric breakdown) test of the gate oxide was typically $15\text{C}/\text{cm}^2$ equivalent to that of a silicon device. The negative gate bias of the commercial SiC MOSFETs is limited to -6 V. This is because continuous negative gate bias causes a negative shift in threshold voltage, possibly due to hole traps in the gate oxide or MOS interface. However, rate of change in threshold voltage of SiC trench MOSFETs under negative gate bias testing at $V_{\text{gs}} = -18\text{V}$ after 3000 hours covered a range of only 5 %.

Fig.11 shows 2 kinds of $I_{\text{d}}-V_{\text{ds}}$ characteristics of the trench MOSFETs using different epilayers: $1.8\text{e}^{16}\text{cm}^{-3}/5\mu\text{m}$ and $7.5\text{e}^{15}\text{cm}^{-3}/7\mu\text{m}$. The die sizes are the same, 2.56mm^2 and the active areas are 1.422mm^2 . The $R_{\text{on,sp}}$ of these was estimated at $0.79\text{m}\Omega\text{cm}^2$ and $1.41\text{m}\Omega\text{cm}^2$ at $I_{\text{d}} = 1\text{A}$, respectively. The blocking voltage of these was 690 V and 1200 V at $I_{\text{d}} = 100\mu\text{A}$, respectively. Fig.12 shows the performance comparison of 4H-SiC switching devices. We could achieve low on-resistance while maintaining the high reliability of the gate oxide.

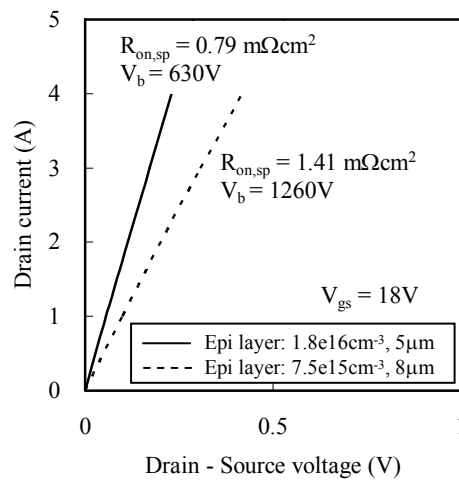


Fig. 11. $I_{\text{d}}-V_{\text{ds}}$ characteristics of double-trench MOSFETs at $V_{\text{gs}} = 18\text{V}$

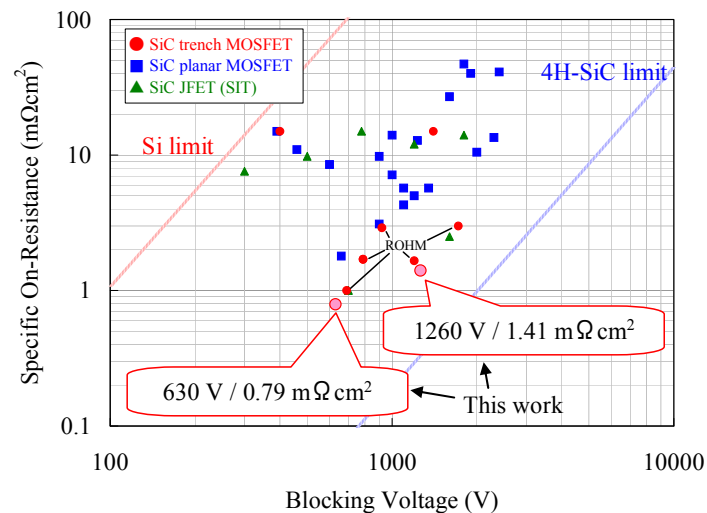


Fig. 12. Performance comparison of 4H-SiC switching device

1.4. Conclusions

Our developed SiC planar MOSFETs have suppressed the degradation of parasitic PN junction diodes when forward current penetrates. SiC Schottky diodes with trench structure successfully showed ultra low forward voltage drop with maintaining low leakage current. SiC MOSFETs with a double-trench structure have obtained ultra low on-resistance with improved reliability of the gate oxide.

2. Literature

- [1] M. Aketa, 2011 International Conference on Silicon Carbide and Related Materials Abstract Book, pp. 258.
- [2] H. Nakao, H. Mikami, H. Yano, T. Hatayama, Y. Uraoka and T. Fuyuki, Mater. Sci. Forum Vol.527-529 (2006), p.1293.
- [3] H. Yano, H. Nakao, T. Hatayama, Y. Uraoka and T. Fuyuki: Mater. Sci. Forum Vol. 556-557 (2007), p. 807
- [4] Y. Nakano, 2011 International Conference on Silicon Carbide and Related Materials Abstract Book, pp. 147.
- [5] T. Nakamura, International Electron Devices Meeting 2011, pp. 599-601.