200-mA 3.3-V or 5.0-V Output LDO Regulators

BD4xxM2-C Series

●General Description

The BD4xxM2-C series are low quiescent regulators featuring 45 V absolute maximum voltage, and output voltage accuracy of ±2 %(3.3 V or 5.0 V: Typ.), 200 mA output current and 40 µA (Typ.) current consumption. These regulators are therefore ideal for applications requiring a direct connection to the battery and a low current consumption.
A logical “HIGH” at the CTL pin enables the device and “LOW” at the CTL pin not enable the device.
(Only W: Includes switch)
Ceramic capacitors can be used for compensation of the output capacitor phase. Furthermore, these ICs also feature overcurrent protection to protect the device from damage caused by short-circuiting and an integrated thermal shutdown to protect the device from overheating at overload conditions.

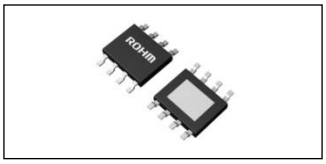
●Features

- Qualified for Automotive Applications
- Wide Temperature Range: -40 °C to +150 °C
- Wide Operating Input Range: 3.0 V to 42 V
- Low Quiescent Current: 40 µA (Typ.)
- Output Current: 200 mA (Typ.)
- High Output Voltage Accuracy: ±2 %
- Output Voltage: 3.3 V or 5.0 V (Typ.)
- Enable Input (Only W: Includes Enable Input)
- Over Current Protection (OCP)
- Thermal Shutdown Protection (TSD)
- AEC-Q100 Qualified

●Packages

W (Typ.) x D (Typ.) x H (Max.)

- EFJ: HTSOP-J8 4.90 mm x 6.00 mm x 1.00 mm
- FP3: SOT223-4F 6.53 mm x 7.00 mm x 1.80 mm



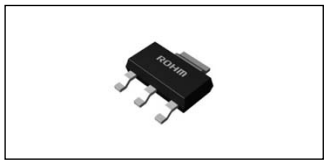


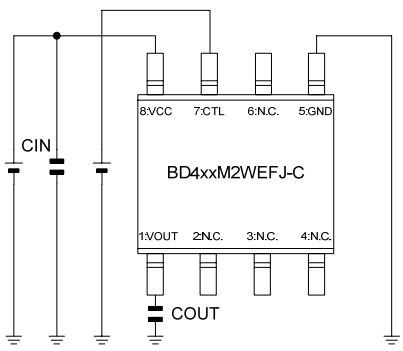
Figure 1. Package Outlook

●Applications

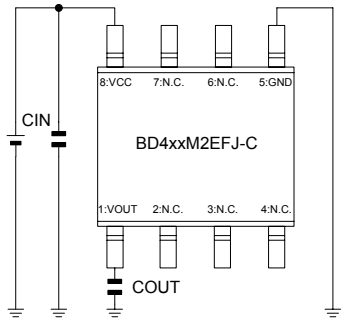
- Automotive
  (body, audio system, navigation system, etc.)

●Typical Application Circuits

- Components externally connected: 0.1 µF ≤ CIN, 10 µF ≤ COUT (Typ.)
  *Electrolytic, tantalum and ceramic capacitors can be used.

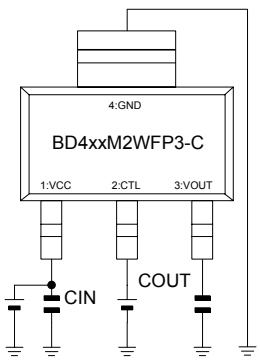


BD433 / 450M2WEFJ-C

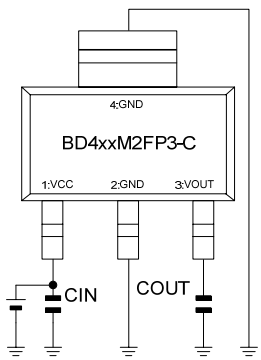


BD433 / 450M2EFJ-C

HTSOP-J8



BD433 / 450M2WFP3-C

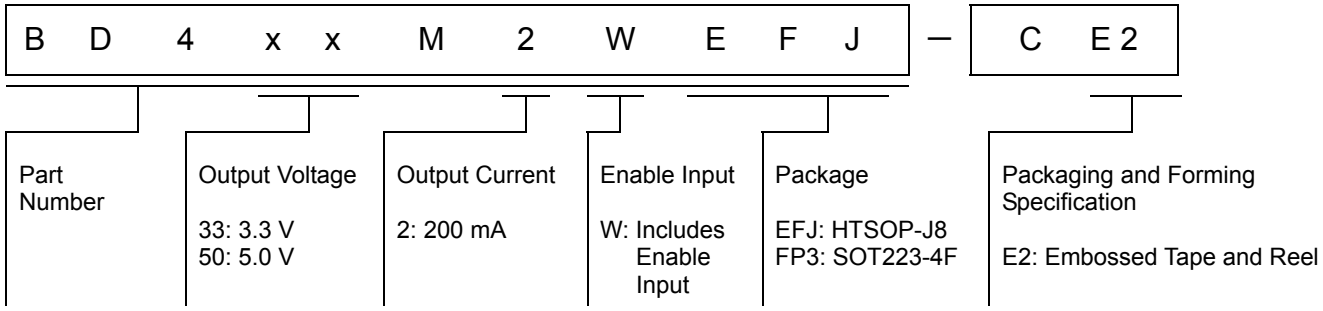


BD433 / 450M2FP3-C

SOT223-4F

Figure 2. Typical Application Circuits

●**Ordering Information**



●**Lineup**

Output Current Ability	Output Voltage (Typ.)	Enable Input *1	Package Type	Orderable Part Number
200 mA	3.3 V	○	SOT223-4F	BD433M2WFP3-CE2
			HTSOP-J8	BD433M2WEFJ-CE2
		–	SOT223-4F	BD433M2FP3-CE2
			HTSOP-J8	BD433M2EFJ-CE2
	5.0 V	○	SOT223-4F	BD450M2WFP3-CE2
			HTSOP-J8	BD450M2WEFJ-CE2
		–	SOT223-4F	BD450M2FP3-CE2
			HTSOP-J8	BD450M2EFJ-CE2

*1 ○: Includes Enable Input.
–: Not includes Enable Input.

●Pin Configurations

Figure 3. Pin Configuration

●Pin Descriptions

■BD433 / 450M2WEFJ-C

Pin No.	Pin Name	Function
1	VOUT	Output pin
2	N.C.	Not Connected
3	N.C.	Not Connected
4	N.C.	Not Connected
5	GND	Ground Pin
6	N.C.	Not Connected
7	CTL	Output Control Pin
8	VCC	Supply Voltage Input Pin

■BD433 / 450M2WFP3-C

Pin No.	Pin Name	Function
1	VCC	Supply Voltage Input Pin
2	CTL	Output Control Pin
3	VOUT	Output Pin
4 (FIN)	GND	Ground Pin

■BD433 / 450M2EFJ-C

Pin No.	Pin Name	Function
1	VOUT	Output Pin
2	N.C.	Not Connected
3	N.C.	Not Connected
4	N.C.	Not Connected
5	GND	Ground Pin
6	N.C.	Not Connected
7	N.C.	Not Connected
8	VCC	Supply Voltage Input Pin

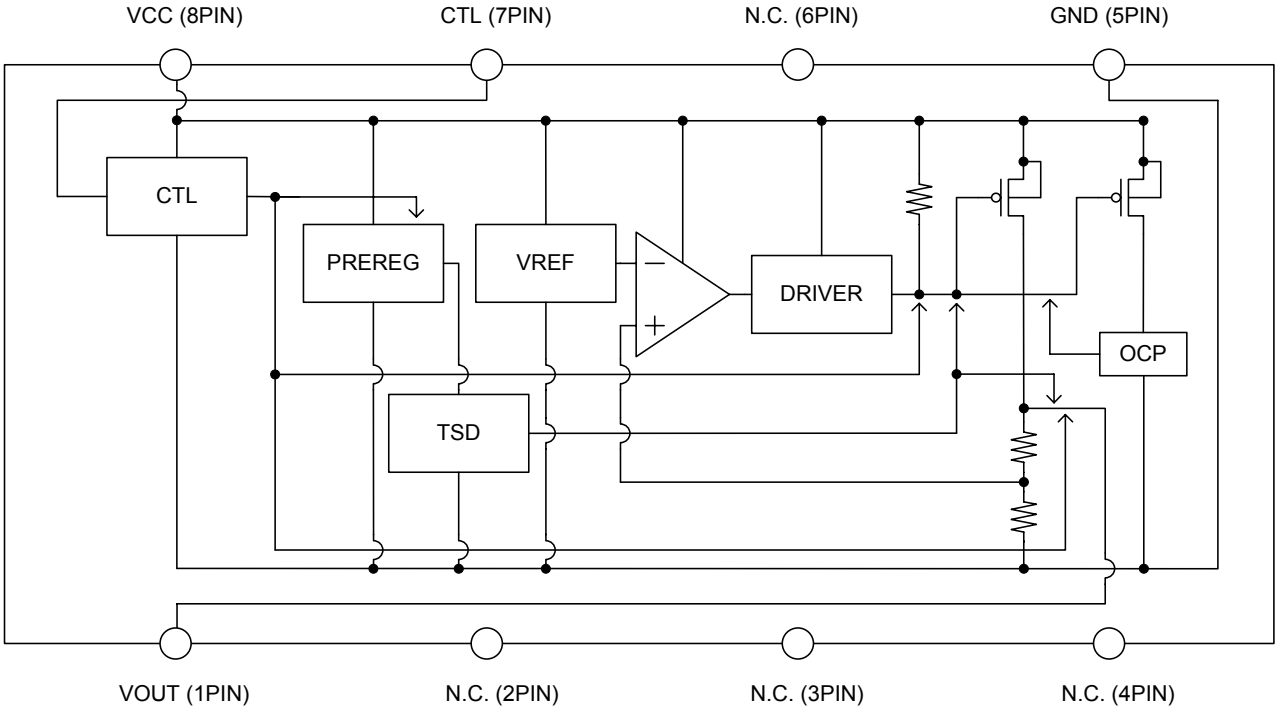
■BD433 / 450M2FP3-C

Pin No.	Pin Name	Function
1	VCC	Supply Voltage Input Pin
2	GND	Ground Pin
3	VOUT	Output Pin
4 (FIN)	GND	Ground Pin

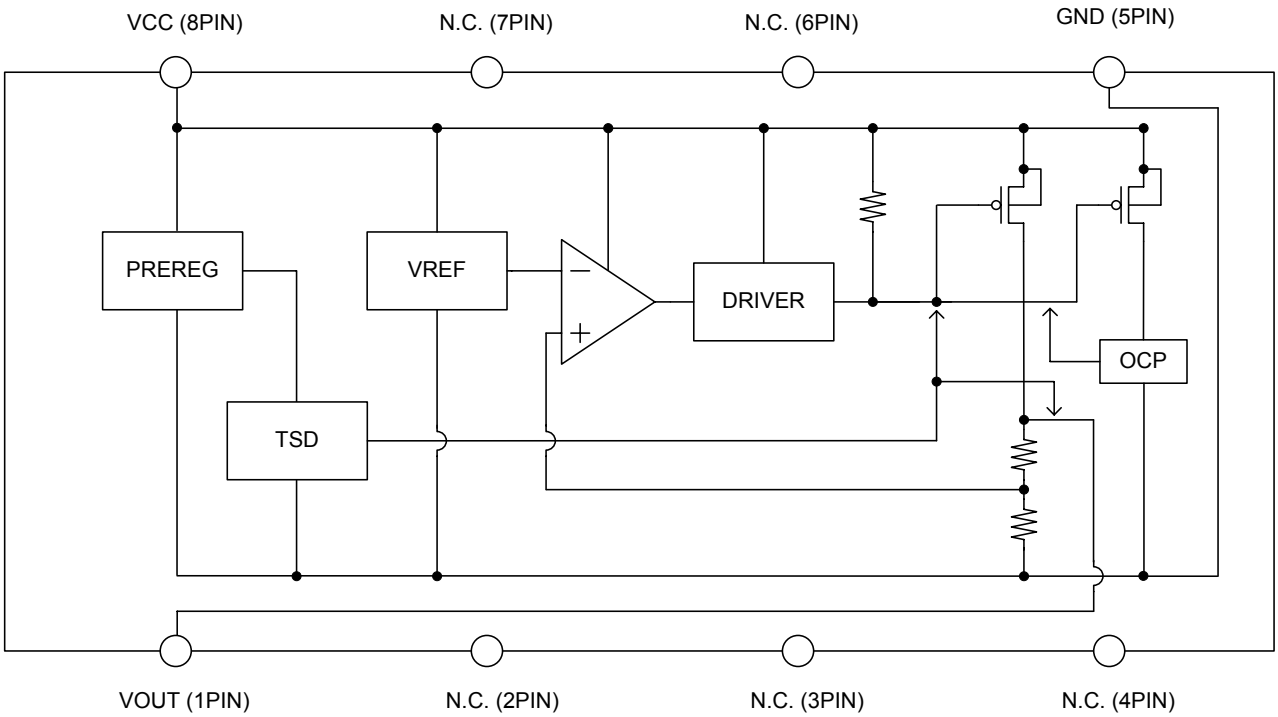
* N.C. Pin is recommended to short with GND.
* N.C. Pin can be open because it isn't connect it inside of IC.
* Exposed die pad is need to be connected to GND.

●Block Diagrams

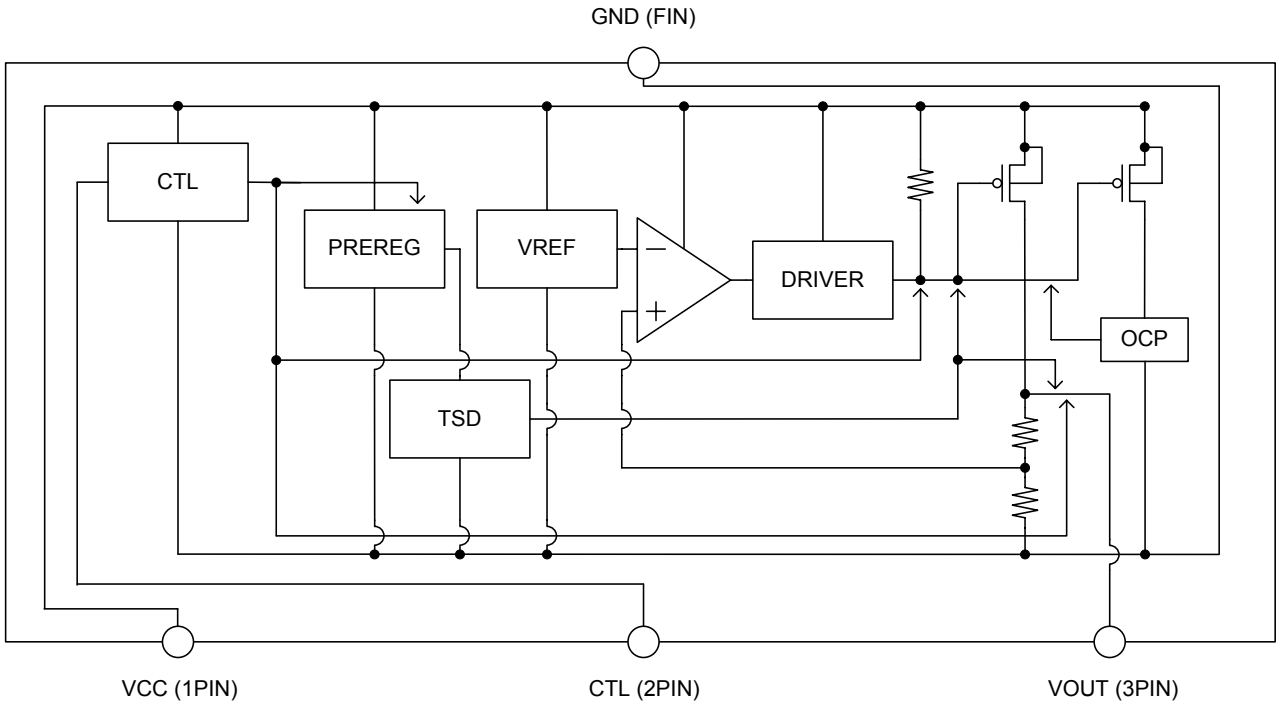
■BD433 / 450M2WEFJ-C



■BD433 / 450M2EFJ-C



■BD433 / 450M2WFP3-C



■BD433 / 450M2FP3-C

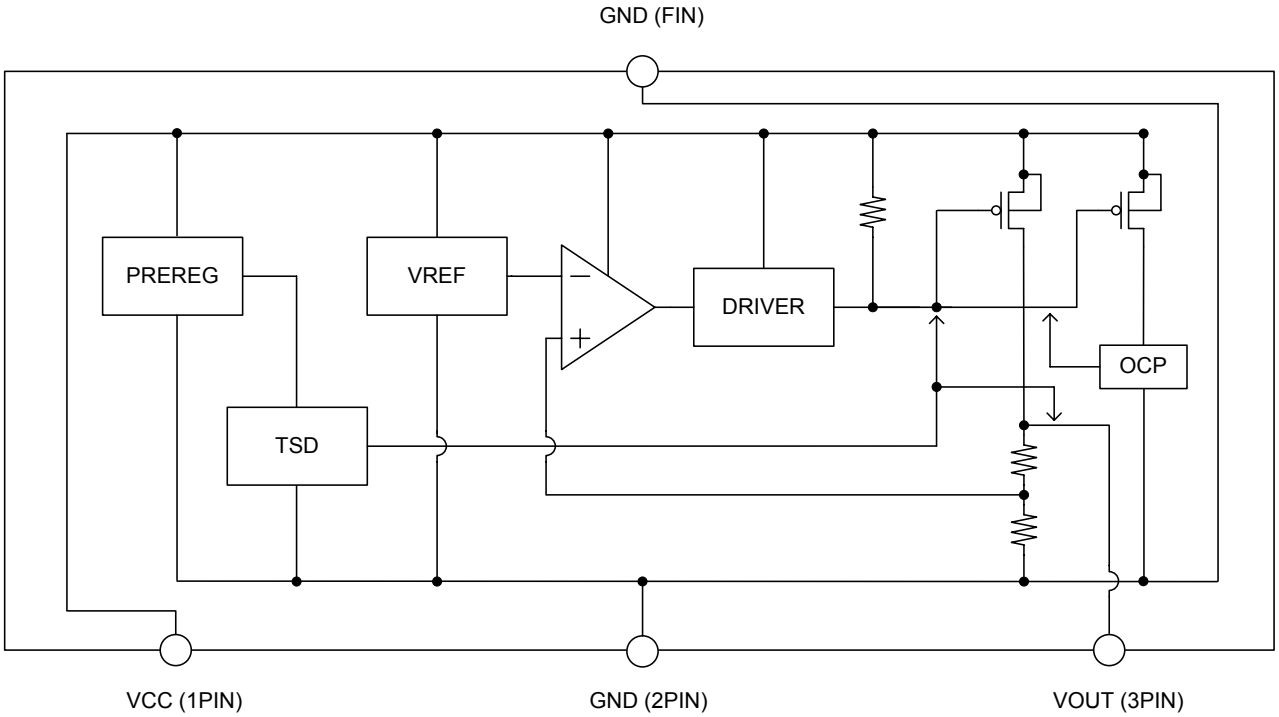


Figure 4. Block Diagrams

●**Description of Blocks**

Brock Name	Function	Description of Blocks
CTL *1	Control Output Voltage ON/OFF	A logical “HIGH” (≥ 2.8 V) at the CTL pin enables the device and “LOW” (≤ 0.8 V) at the CTL pin not enable the device.
PREREG	Internal Power Supply	Power Supply for Internal Circuit
TSD	Thermal Shutdown Protection	To protect the device from overheating. If the chip temperature (Tj) reaches ca. 175 °C (Typ.), the output is turned off.
VREF	Reference Voltage	Generate the Reference Voltage
DRIVER	Output MOS FET Driver	Drive the Output MOS FET
OCP	Over Current Protection	To protect the device from damage caused by over current. If the output current reaches ca. 550 mA (Typ.), The output is turned off.

*1 Applicable for product with Enable Input.

●Absolute Maximum Ratings

Parameter			Symbol	Ratings	Unit
Supply Voltage		*1	VCC	-0.3 to +45.0	V
Output Control Voltage		*2	CTL	-0.3 to +45.0	V
Output Voltage			VOUT	-0.3 to +8.0	V
Power Dissipation	HTSOP-J8	*3	Pd	0.75	W
	SOT223-4F	*3	Pd	0.60	W
Junction Temperature Range			Tj	-40 to +150	°C
Storage Temperature Range			Tstg	-55 to +150	°C
Maximum Junction Temperature			Tjmax	+150	°C
ESD withstand Voltage (HBM)		*4	$V_{ESD,HBM}$	±2000	V

*1 Do not exceed Pd.
*2 Applicable for product with Enable Input.
The start up orders of power supply (VCC) and the CTL pin do not influence if the voltage is within the operation power supply voltage range.
*3 HTSOP-J8 mounted on 114.3 mm x 76.2 mm x 1.6 mmt Glass-Epoxy PCB based on JEDEC. If Ta ≧25 °C, reduce by 6.0 mW/°C.
(1-layer PCB: Copper foil area on the reverse side of PCB:0 mm x 0 mm)
SOT223-4F mounted on 114.3 mm x 76.2 mm x 1.6 mmt Glass-Epoxy PCB based on JEDEC. If Ta ≧25 °C, reduce by 4.8 mW/°C.
(1-layer PCB: Copper foil area on the reverse side of PCB:0 mm x 0 mm)

*4 ESD susceptibility Human Body Model “HBM”

●Operating Conditions (-40 °C ≤ Tj ≤ +150 °C)

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage (IOUT ≤ 200 mA)	*1	VCC	4.3	42.0	V
Supply Voltage (IOUT ≤ 100 mA)	*1	VCC	3.9	42.0	V
Supply Voltage (IOUT ≤ 200 mA)	*2	VCC	5.8	42.0	V
Supply Voltage (IOUT ≤ 100 mA)	*2	VCC	5.5	42.0	V
Output Control Voltage	*3	CTL	0	42.0	V
Start-Up Voltage	*4	VCC	3.0	—	V
Output Current		IOUT	0	200	mA
Junction Temperature Range		Tj	-40	+150	°C

*1 BD433M2WEFJ-C / BD433M2WFP3-C / BD433M2EFJ-C / BD433M2FP3-C
*2 BD450M2WEFJ-C / BD450M2WFP3-C / BD450M2EFJ-C / BD450M2FP3-C
*3 Applicable for product with Enable Input
*4 When IOUT = 0 mA

●**Thermal Resistance**

Parameter		Symbol	Min.	Max.	Unit
HTSOP-J8 Package					
Junction to Ambient	*1	θja	43.1	—	°C/W
Junction to Case (bottom)	*1	θjc	10	—	°C/W
SOT223-4F Package					
Junction to Ambient	*2	θja	83.3	—	°C/W
Junction to Case (bottom)	*2	θjc	17	—	°C/W

*1 HTSOP-J8 mounted on 114.3 mm x 76.2 mm x 1.6 mmt Glass-Epoxy PCB based on JEDEC.
(4-layer PCB: Copper foil on the reverse side of PCB:74.2 mm x 74.2 mm)

*2 SOT223-4F mounted on 114.3 mm x 76.2 mm x 1.6 mmt Glass-Epoxy PCB based on JEDEC.
(4-layer PCB: Copper foil on the reverse side of PCB:74.2 mm x 74.2 mm)

●Electrical Characteristics

(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V(*1), IOUT = 0 mA.
The Typical value is defined at Tj = 25 °C.)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Shut Down Current	Ishut *1	—	2.0	5.0	μA	CTL = 0 V, Tj ≤ 125 °C
Circuit Current	Icc	—	40	90	μA	IOUT = 0 mA, Tj ≤ 125 °C
		—	40	150	μA	IOUT ≤ 200 mA, Tj ≤ 150 °C
Output Voltage	VOUT *2	4.90	5.00	5.10	V	6 V ≤ VCC ≤ 42 V, 0 mA ≤ IOUT ≤ 50 mA
		4.80	5.00	5.10	V	6 V ≤ VCC ≤ 42 V, IOUT ≤ 200 mA
	VOUT *3	3.23	3.30	3.37	V	6 V ≤ VCC ≤ 42 V, 0 mA ≤ IOUT ≤ 50 mA
		3.16	3.30	3.37	V	6 V ≤ VCC ≤ 42 V, IOUT ≤ 200 mA
Dropout Voltage	ΔVd *2	—	0.16	0.35	V	VCC = VOUT x 0.95 (= 4.75V: Typ.), IOUT = 100 mA
	ΔVd *3	—	0.20	0.45	V	VCC = VOUT x 0.95 (= 3.135V: Typ.), IOUT = 100 mA
Ripple Rejection	R.R.	55	65	—	dB	f = 120 Hz, ein = 1 Vrms, IOUT = 100 mA
Line Regulation	Reg.I	—	10	30	mV	VCC = 8 V → 16 V
Load Regulation	Reg.L	—	10	30	mV	IOUT = 10 mA → 100 mA
Thermal Shut Down	TSD	—	175	—	°C	Tj at TSD ON

*1 Applicable for product with Enable Input.
*2 For BD450M2WEFJ-C / BD450M2WFP3-C / BD450M2EFJ-C / BD450M2FP3-C
*3 For BD433M2WEFJ-C / BD433M2WFP3-C / BD433M2EFJ-C / BD433M2FP3-C

●Electrical Characteristics (Enable function * Applicable for product with Enable Input.)

(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, IOUT = 0 mA. The Typical value is defined at Tj = 25 °C.)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
CTL ON Mode Voltage	VthH	2.8	—	—	V	ACTIVE MODE
CTL OFF Mode Voltage	VthL	—	—	0.8	V	OFF MODE
CTL Bias Current	ICTL	—	15	30	μA	CTL = 5 V

●**Typical Performance Curves**

■BD433M2WEFJ-C / BD433M2EFJ-C / BD433M2WFP3-C / BD433M2FP3-C Reference Data

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V (*1), IOUT = 0 mA.

*1 Applicable for product with Enable Input.

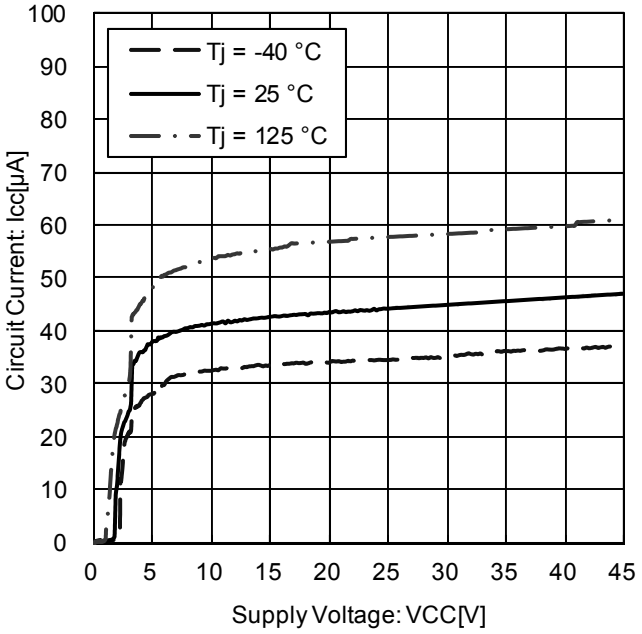


Figure 5. Circuit Current vs. Power Supply Voltage

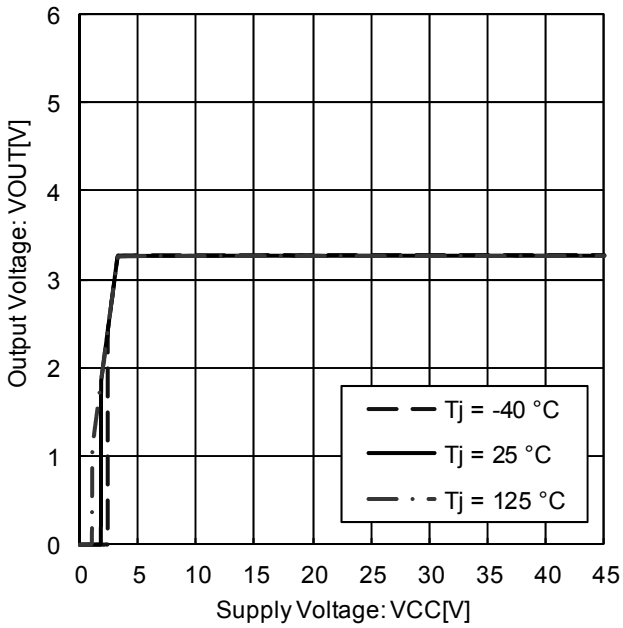


Figure 6. Output Voltage vs. Power Supply Voltage (IOUT = 0 mA)

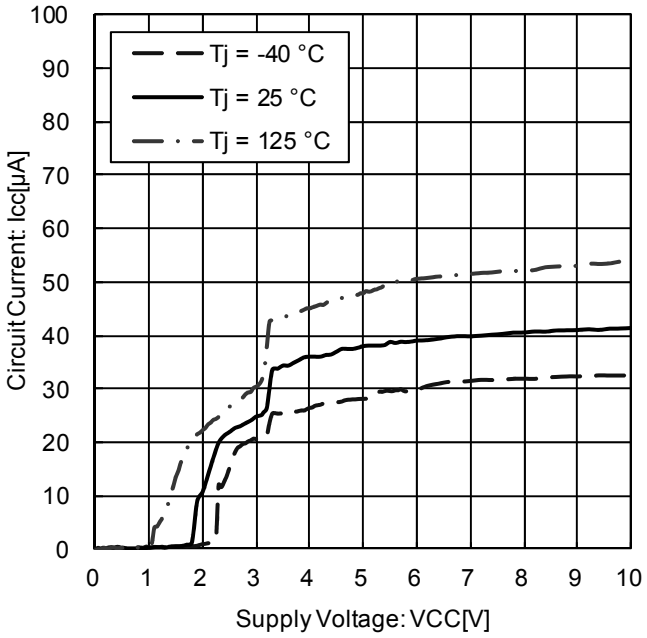


Figure 7. Circuit Current vs. Power Supply Voltage
*magnified Figure 5. at low supply voltage

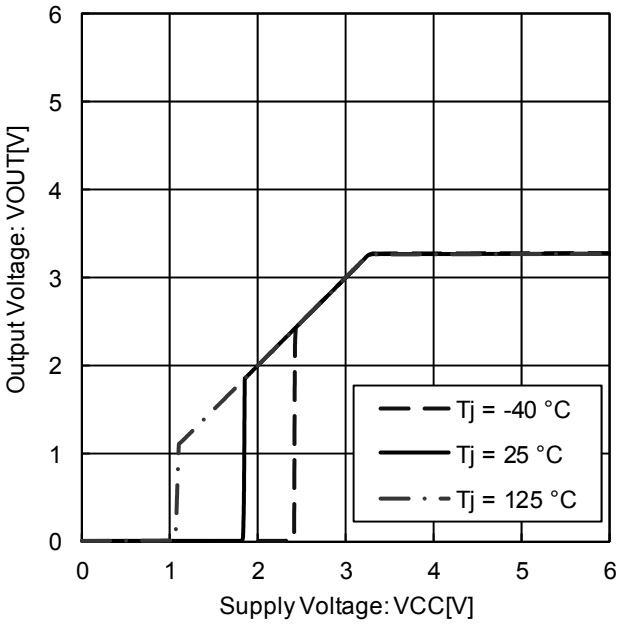


Figure 8. Output Voltage vs. Power Supply Voltage (IOUT = 0 mA)
*magnified Figure 6. at low supply voltage

●**Typical Performance Curves**

■BD433M2WEFJ-C / BD433M2EFJ-C / BD433M2WFP3-C / BD433M2FP3-C Reference Data

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V (*1), IOUT = 0 mA.

*1 Applicable for product with Enable Input.

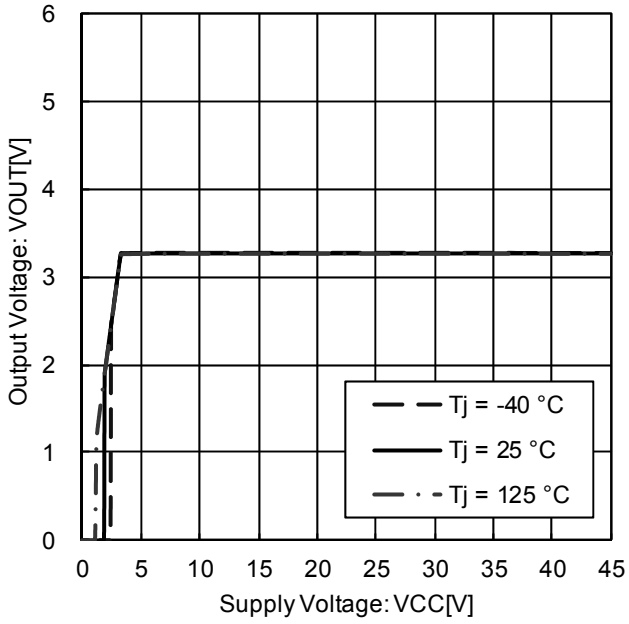


Figure 9. Output Voltage vs. Power Supply Voltage
(IOUT = 10 mA)

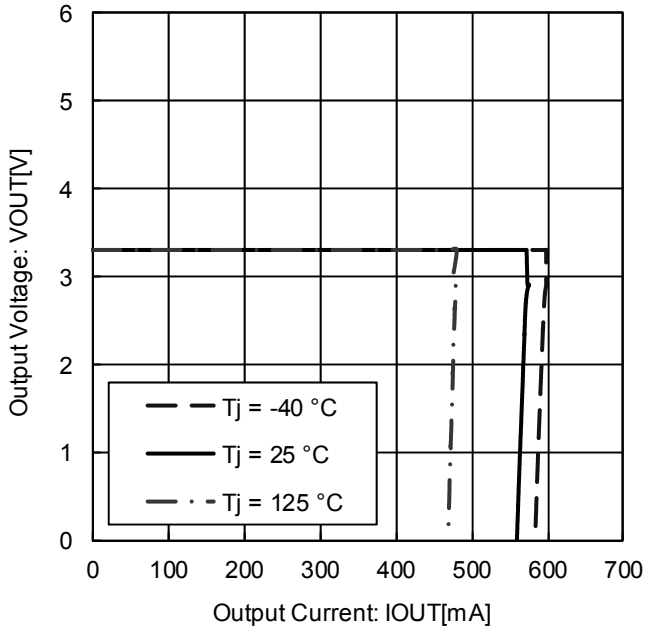


Figure10. Output Voltage vs. Output Current
(Over Current Protection)

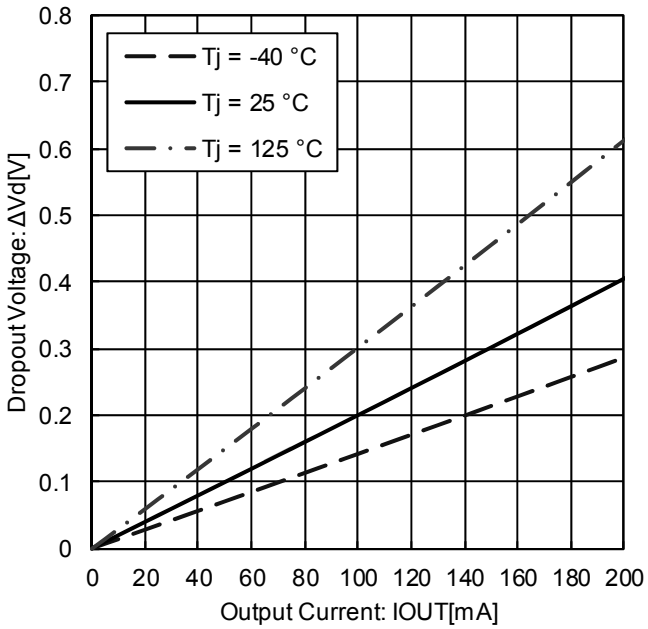


Figure 11. Dropout Voltage
(VCC = 3.135 V)

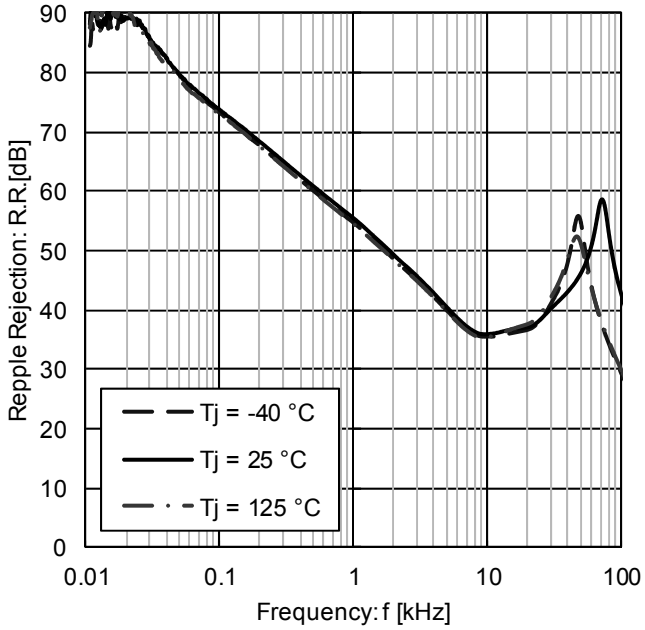


Figure 12. Ripple Rejection
(ein = 1 Vrms, IOUT = 100 mA)

●**Typical Performance Curves**

■BD433M2WEFJ-C / BD433M2EFJ-C / BD433M2WFP3-C / BD433M2FP3-C Reference Data

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V (*1), IOUT = 0 mA.

*1 Applicable for product with Enable Input.

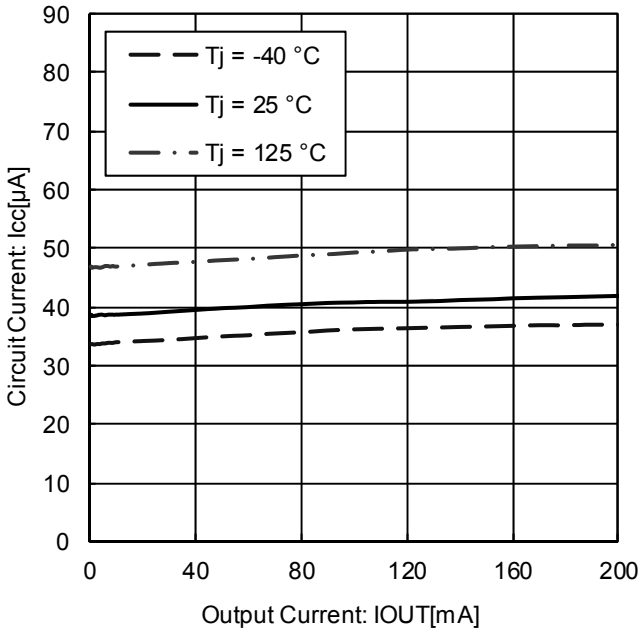


Figure 13. Circuit Current vs. Output Current

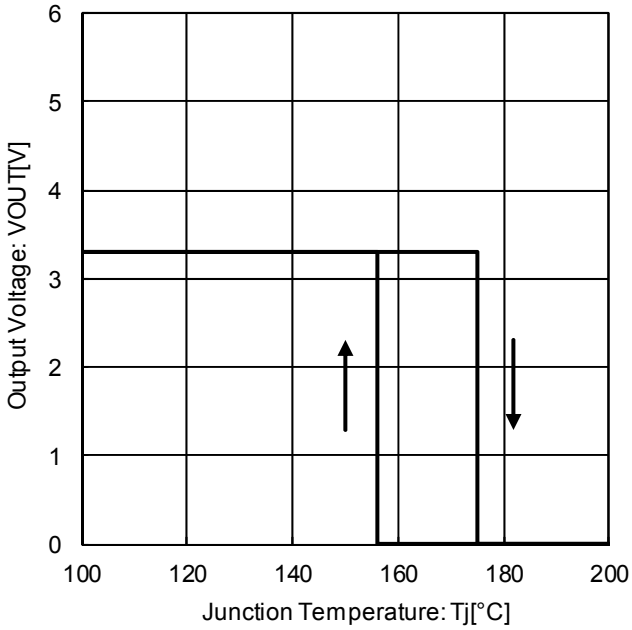


Figure 14. Output Voltage vs. Temperature
(Thermal Shut Down)

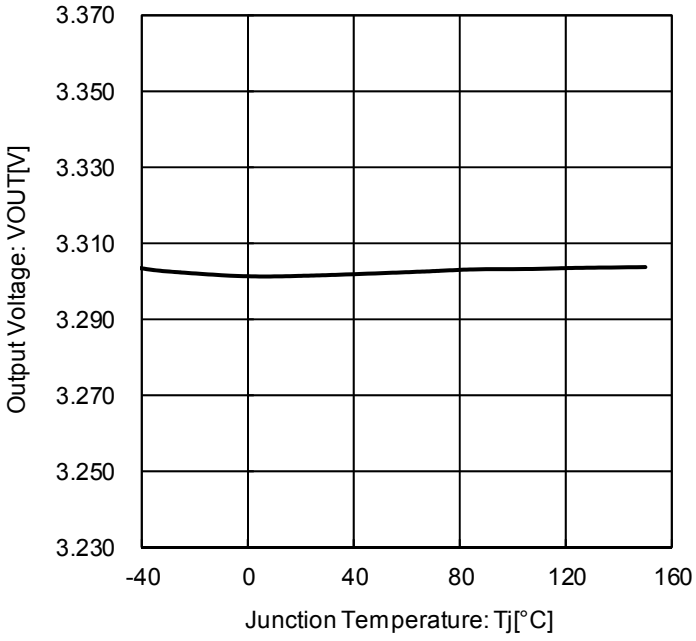


Figure 15. Output Voltage vs. Temperature

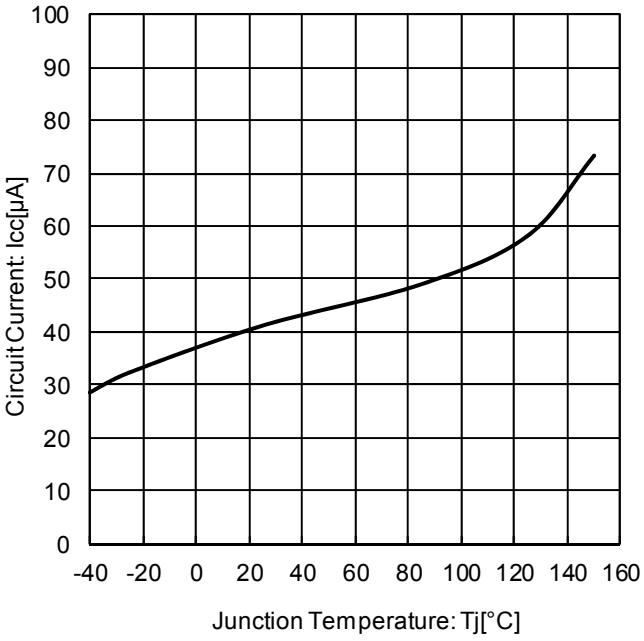


Figure 16. Circuit Current vs. Temperature

●**Typical Performance Curves**

■BD433M2WEFJ-C / BD433M2WFP3-C Reference Data

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, IOUT = 0 mA

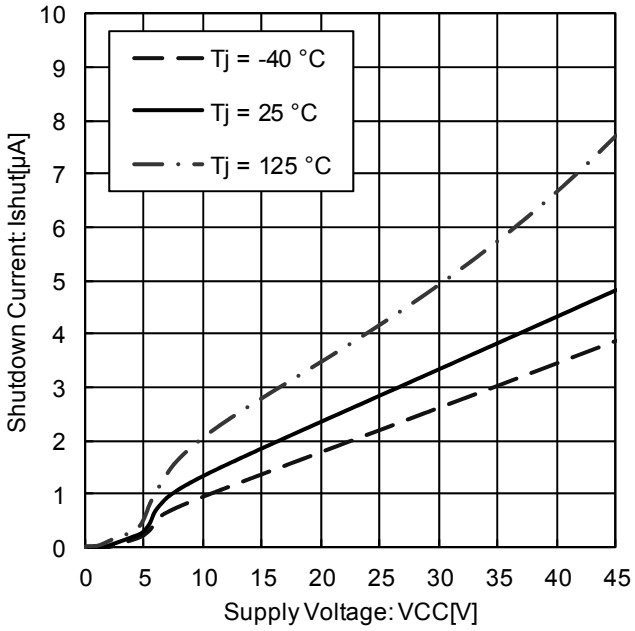


Figure 17. Shut Down Current vs. Power Supply Voltage
(CTL = 0 V)

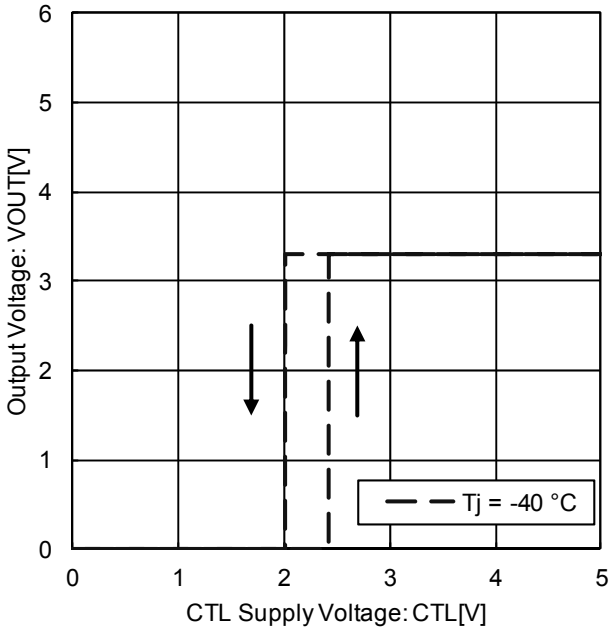


Figure 18. CTL ON / OFF Mode Voltage
(Tj = -40 °C)

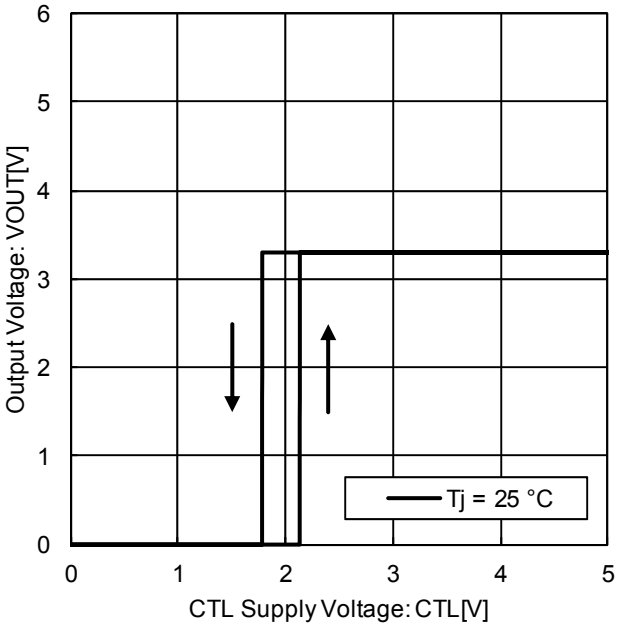


Figure 19. CTL ON / OFF Mode Voltage
(Tj = 25 °C)

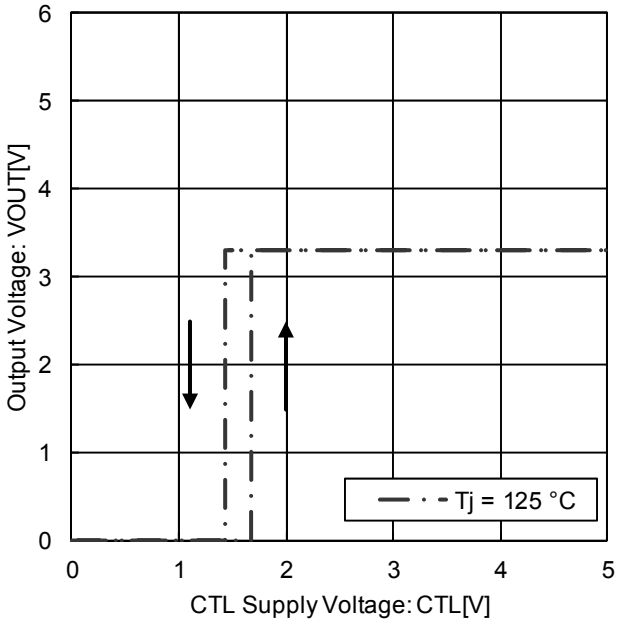


Figure 20. CTL ON / OFF Mode Voltage
(Tj = 125 °C)

●**Typical Performance Curves**

■BD433M2WEFJ-C / BD433M2WFP3-C Reference Data

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, IOUT = 0 mA

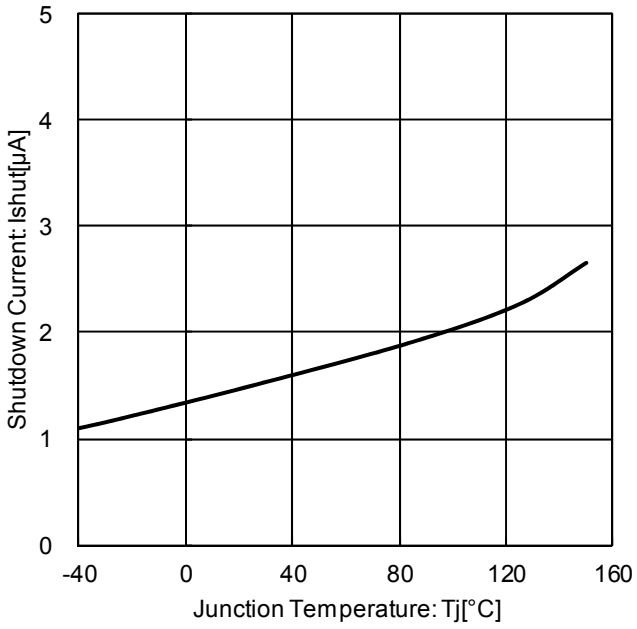


Figure 21. Shut Down Current vs. Temperature (CTL = 0 V)

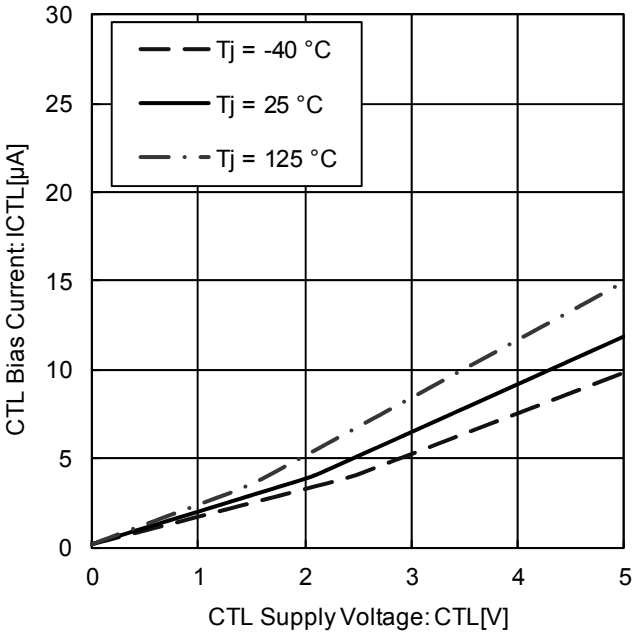


Figure 22. CTL Bias Current vs. CTL Supply Voltage

●**Typical Performance Curves**

■BD450M2WEFJ-C / BD450M2EFJ-C / BD450M2WFP3-C / BD450M2FP3-C Reference Data

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5V (*1), IOUT = 0 mA

*1 Applicable for product with Enable Input.

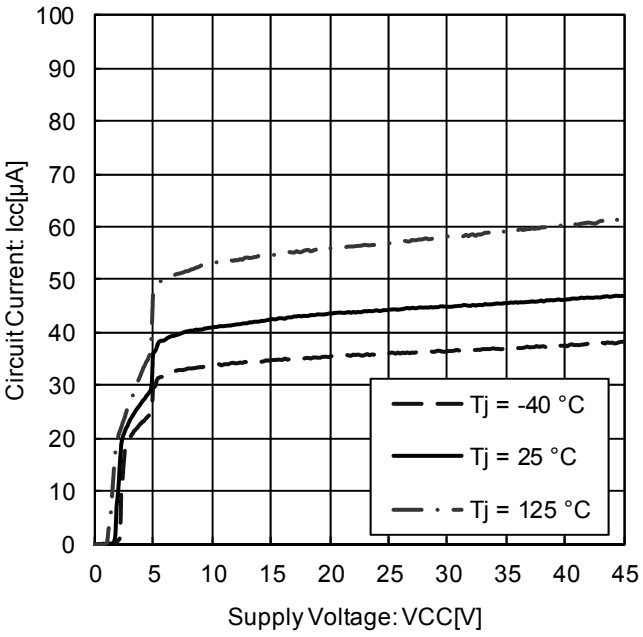


Figure 23. Circuit Current vs. Power Supply Voltage

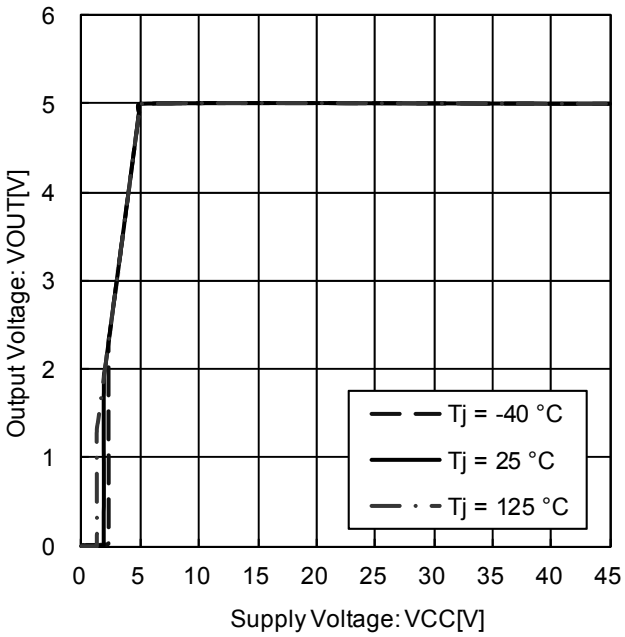


Figure 24. Output Voltage vs. Power Supply Voltage (IOUT = 0 mA)

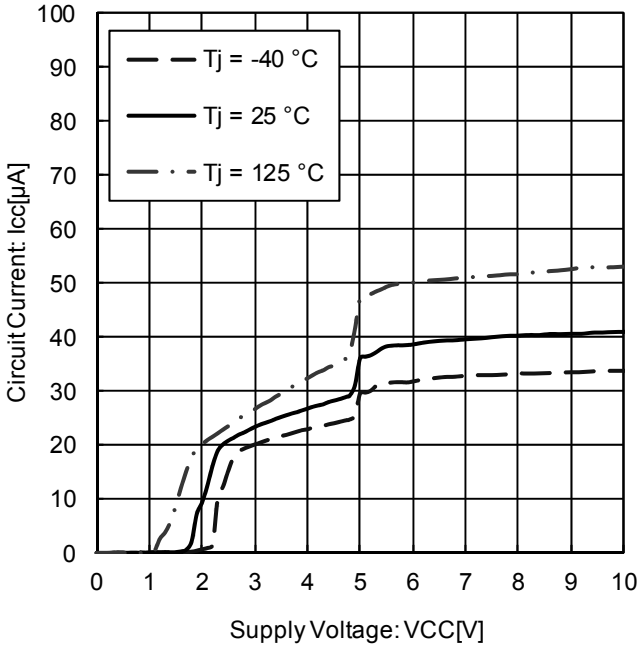


Figure 25. Circuit Current vs. Power Supply Voltage
*magnified Figure 23. at low supply voltage

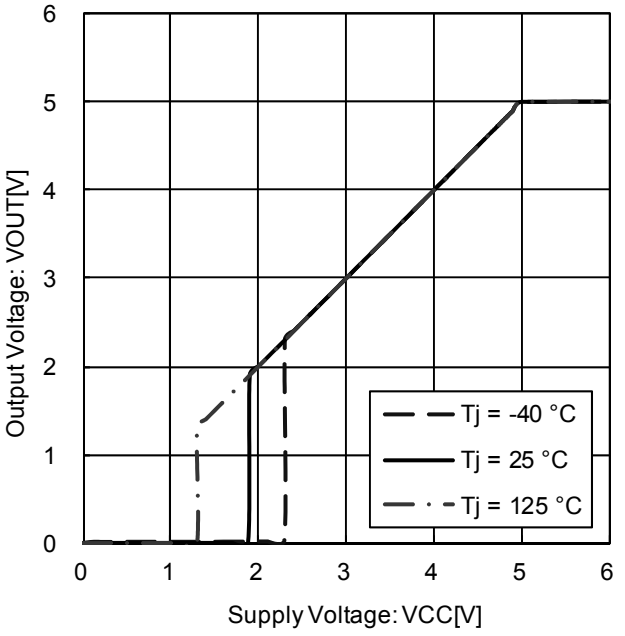


Figure 26. Output Voltage vs. Power Supply Voltage (IOUT = 0 mA)
*magnified Figure 24. at low supply voltage

●**Typical Performance Curves**

■BD450M2WEFJ-C / BD450M2EFJ-C / BD450M2WFP3-C / BD450M2FP3-C Reference Data

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5V (*1), IOUT = 0 mA

*1 Applicable for product with Enable Input.

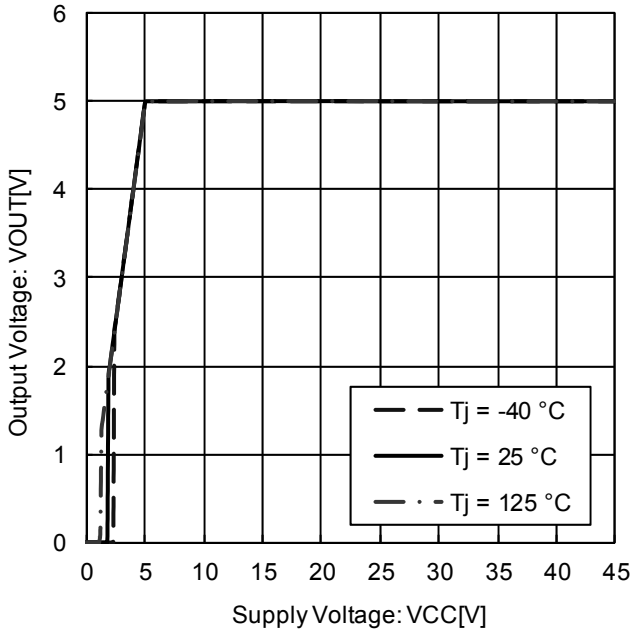


Figure 27. Output Voltage vs. Power Supply Voltage (IOUT = 10 mA)

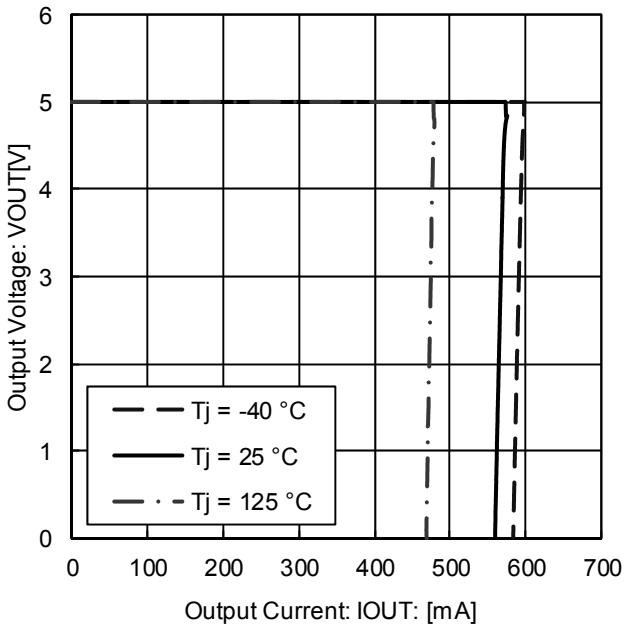


Figure 28. Output Voltage vs. Output Current (Over Current Protection)

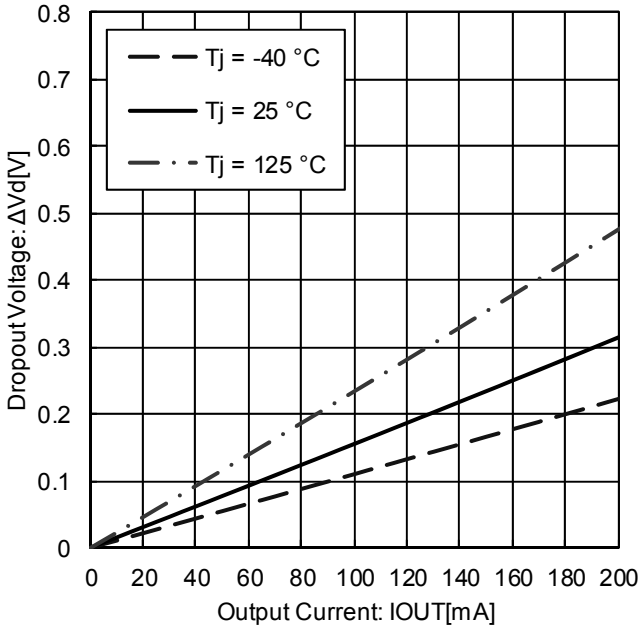


Figure 29. Dropout Voltage (VCC = 4.75 V)

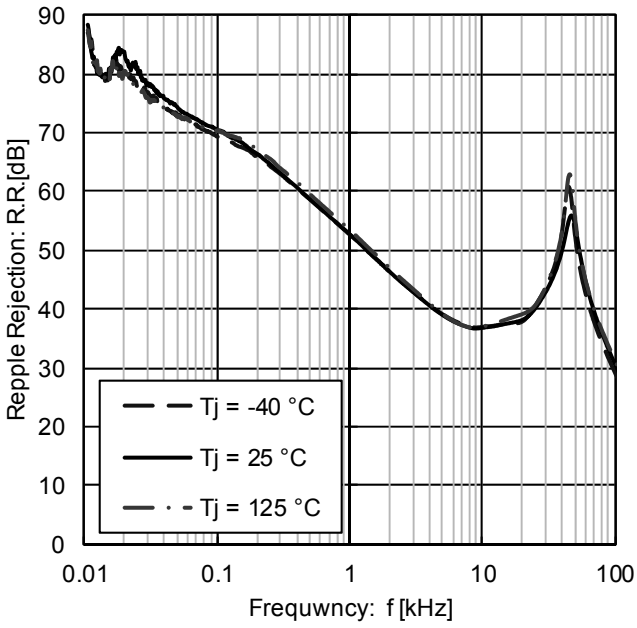


Figure 30. Ripple Rejection (ein = 1 Vrms, IOUT = 100 mA)

●**Typical Performance Curves**

■BD450M2WEFJ-C / BD450M2EFJ-C / BD450M2WFP3-C / BD450M2FP3-C Reference Data

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5V (*1), IOUT = 0 mA

*1 Applicable for product with Enable Input.

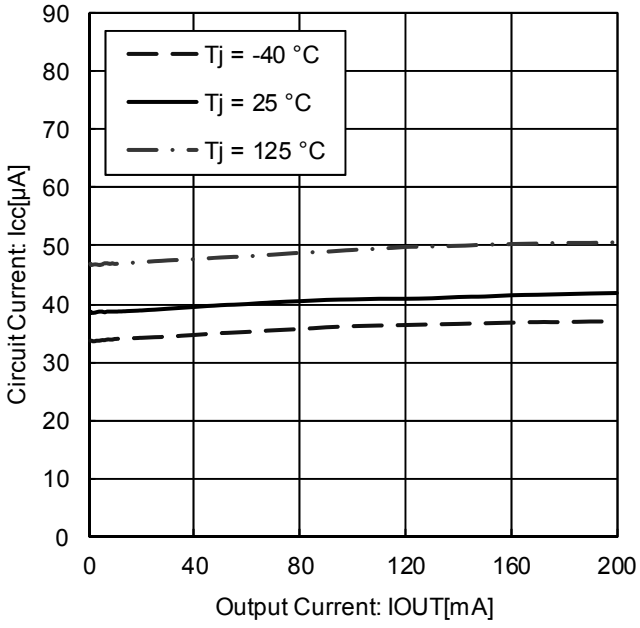


Figure 31. Circuit Current vs. Output Current

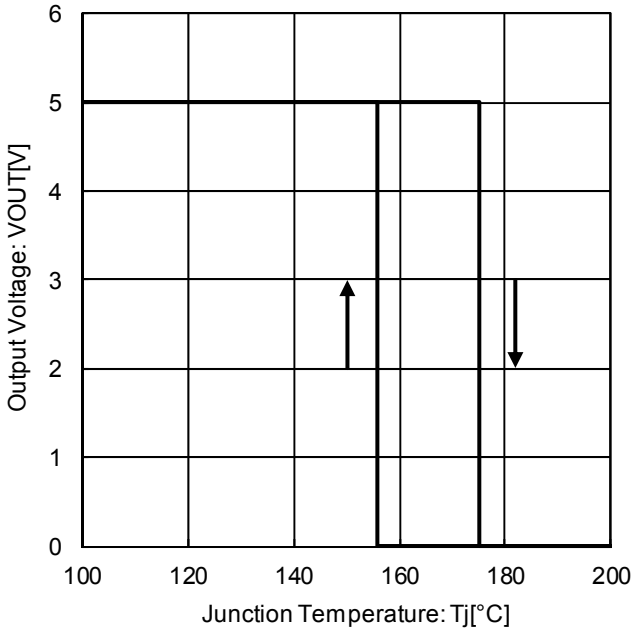


Figure 32. Output Voltage vs. Temperature (Thermal Shut Down)

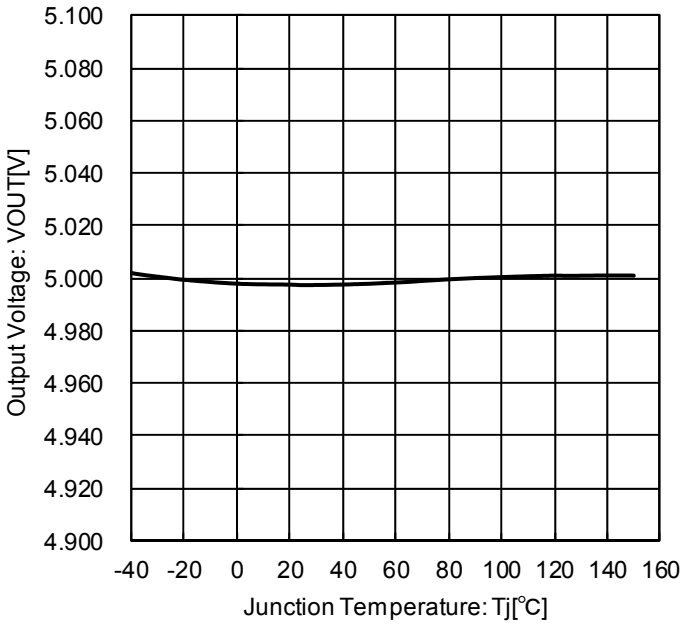


Figure 33. Output Voltage vs. Temperature

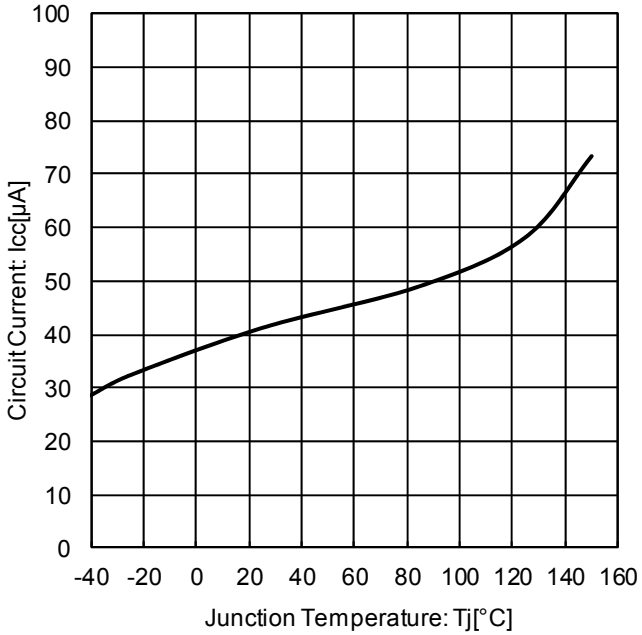


Figure 34. Circuit Current vs. Temperature

●**Typical Performance Curves**

■BD450M2WEFJ-C / BD450M2WFP3-C Reference Data

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, IOUT = 0 mA

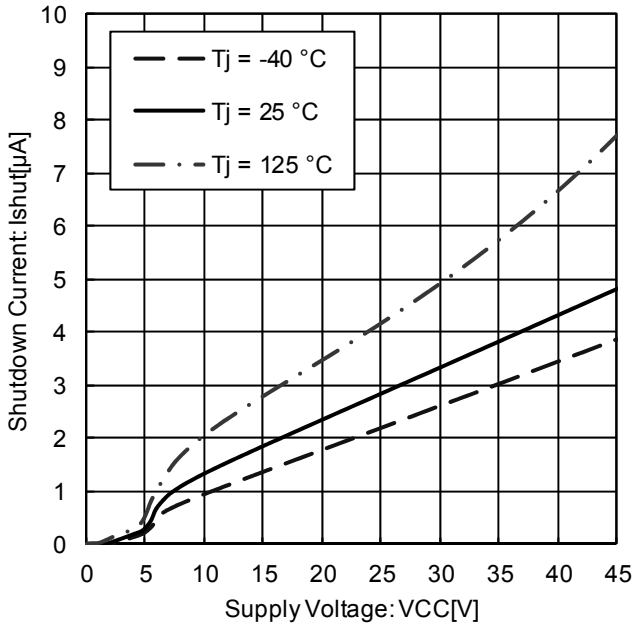


Figure 35. Shut Down Current vs. Power Supply Voltage
(CTL = 0 V)

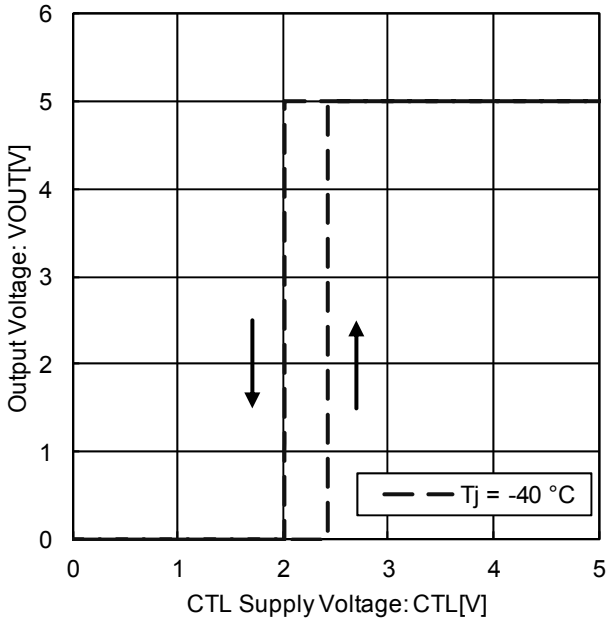


Figure 36. CTL ON / OFF Mode Voltage
(Tj = -40 °C)

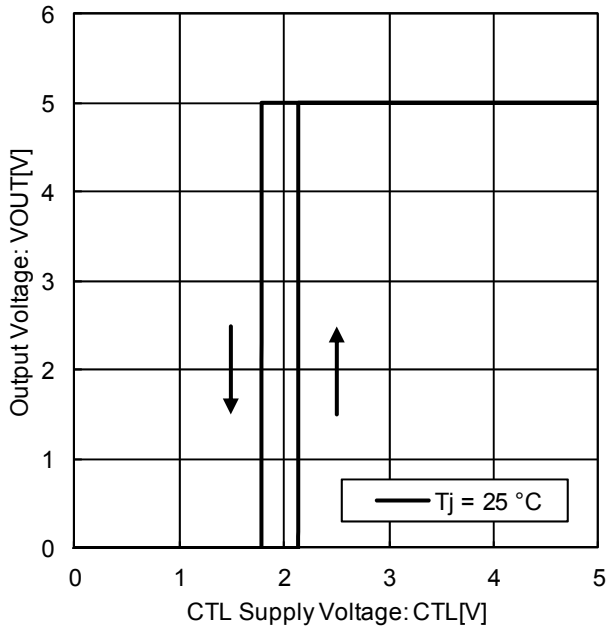


Figure 37. CTL ON / OFF Mode Voltage
(Tj = 25 °C)

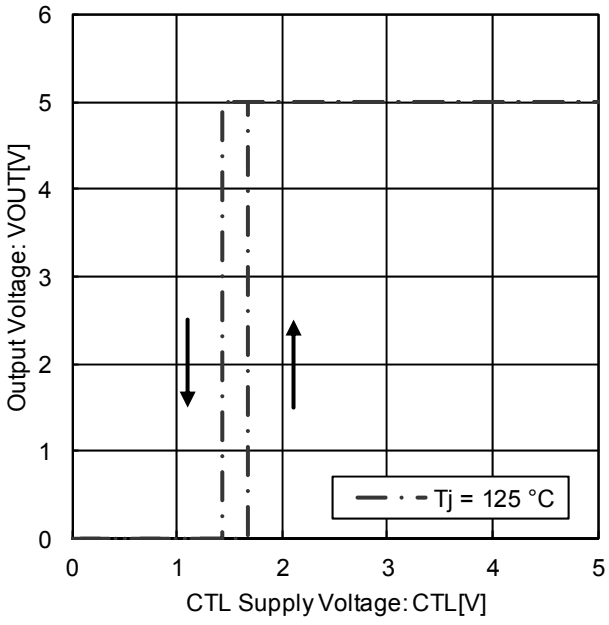


Figure 38. CTL ON / OFF Mode Voltage
(Tj = 125 °C)

●**Typical Performance Curves**

■BD450M2WEFJ-C / BD450M2WFP3-C Reference Data

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, IOUT = 0 mA

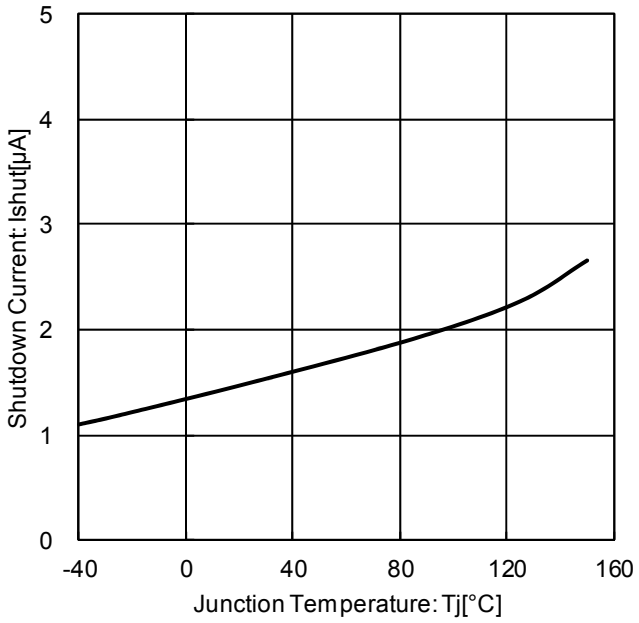


Figure 39. Shut Down Current vs. Temperature
(CTL = 0 V)

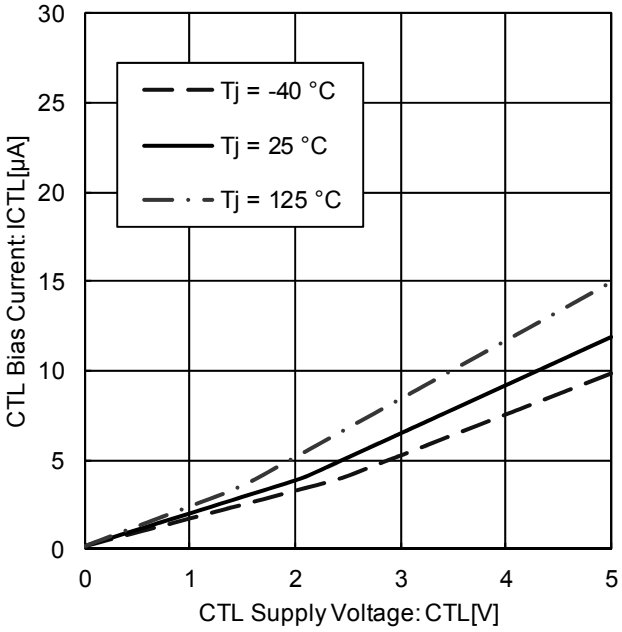
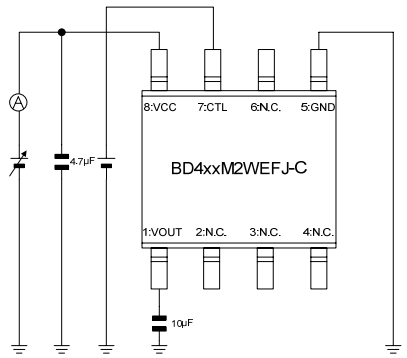
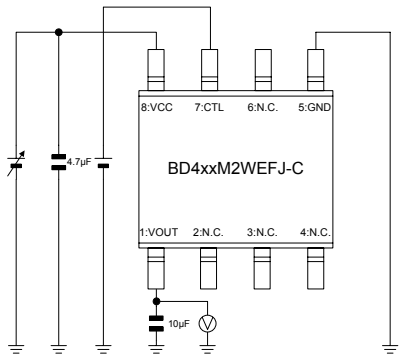


Figure 40. CTL Bias Current vs. CTL Supply Voltage

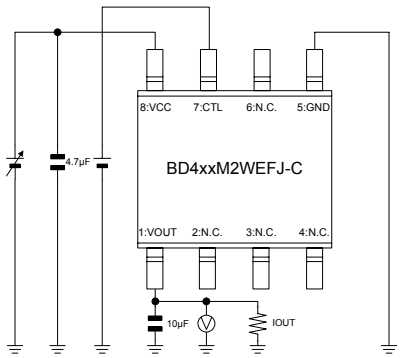
●Measurement Circuit for Typical Performance Curves (BD433 / 450M2WEFJ-C)



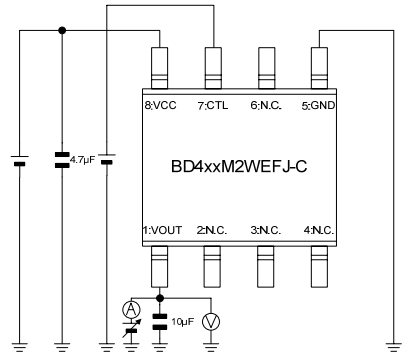
Measurement Setup for
Figure 5, 7, 16, 17, 21,
Figure 23, 25, 34, 35, 39



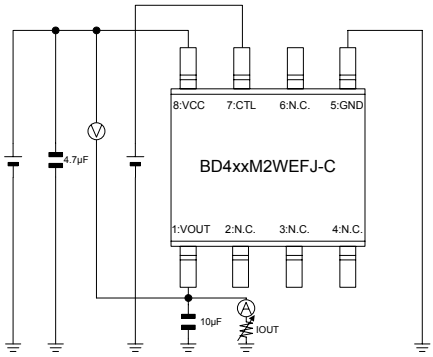
Measurement Setup for
Figure 6, 8, 14, 15,
Figure 24, 26, 32, 33



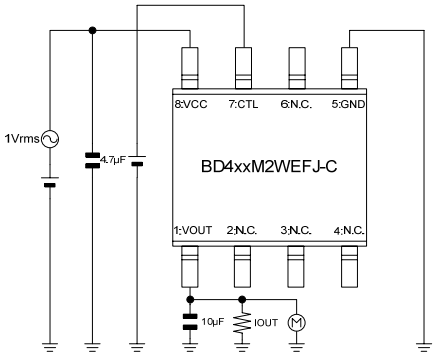
Measurement Setup for
Figure 9, 27



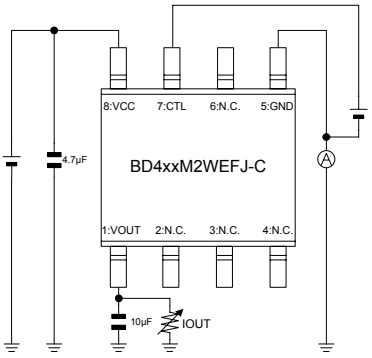
Measurement Setup for
Figure 10, 28



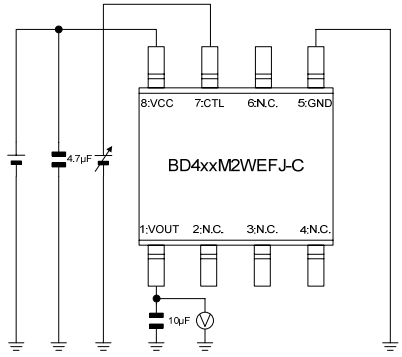
Measurement Setup for
Figure 11, 29



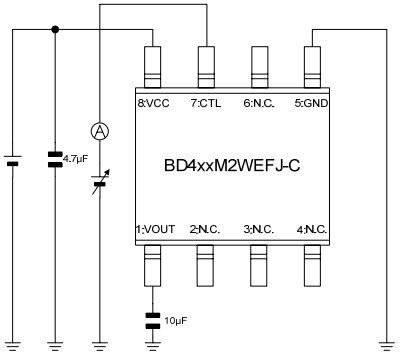
Measurement Setup for
Figure 12, 30



Measurement Setup for
Figure 13, 31

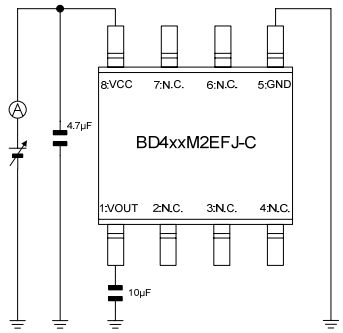


Measurement Setup for
Figure 18, 19, 20,
Figure 36, 37, 38

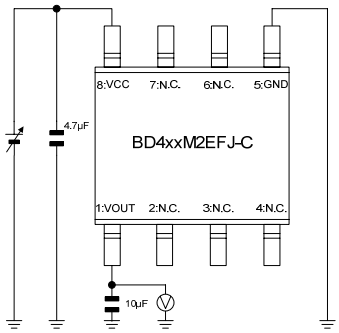


Measurement Setup for
Figure 22, 40

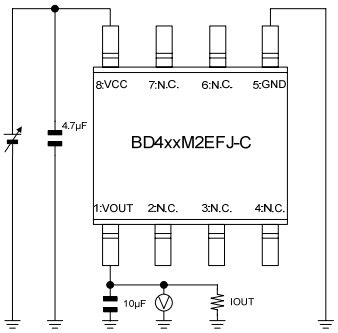
●Measurement Circuit for Typical Performance Curves (BD433 / 450M2EFJ-C)



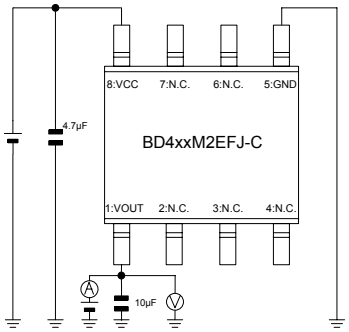
Measurement Setup for
Figure 5, 7, 16,
Figure 23, 25, 34



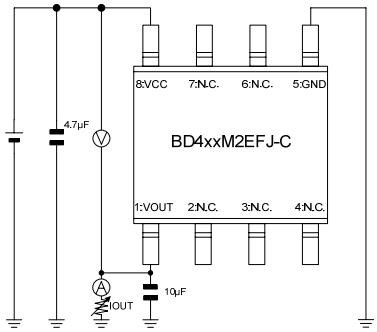
Measurement Setup for
Figure 6, 8, 14, 15,
Figure 24, 26, 32, 33



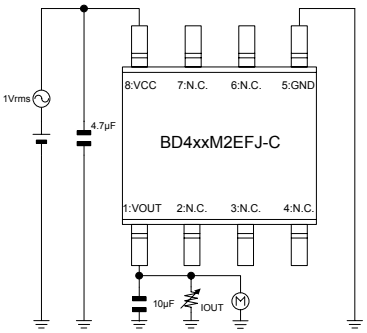
Measurement Setup for
Figure 9, 27



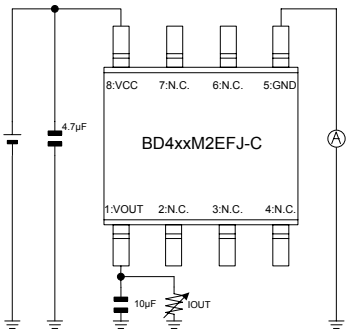
Measurement Setup for
Figure 10, 28



Measurement Setup for
Figure 11, 29

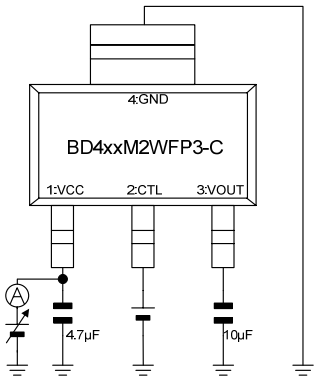


Measurement Setup for
Figure 12, 30

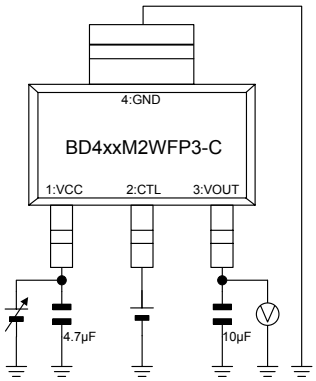


Measurement Setup for
Figure 13, 31

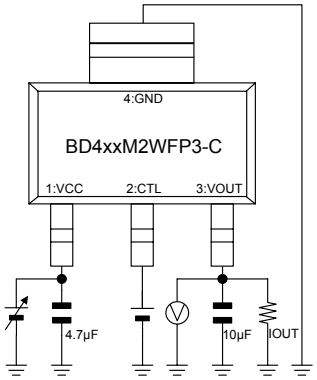
●**Measurement Circuit for Typical Performance Curves (BD433 / 450M2WFP3-C)**



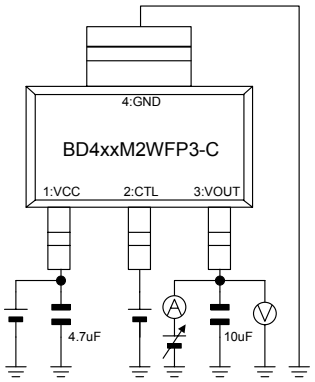
Measurement Setup for
Figure 5, 7, 16, 17, 21,
Figure 23, 25, 34, 35, 39



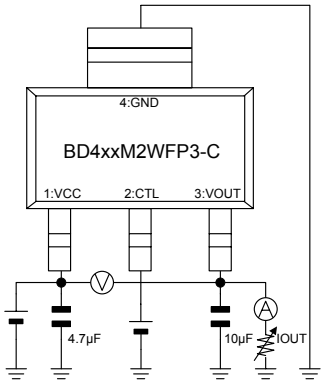
Measurement Setup for
Figure 6, 8, 14, 15,
Figure 24, 26, 32, 33



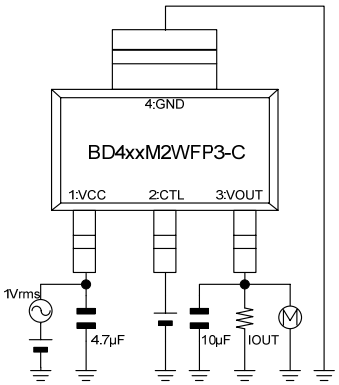
Measurement Setup for
Figure 9, 27



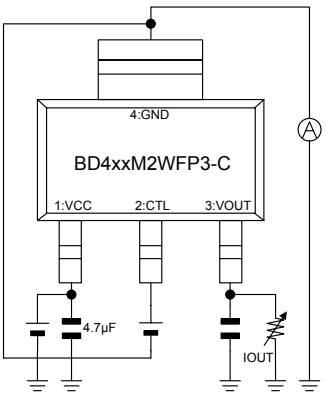
Measurement Setup for
Figure 10, 28



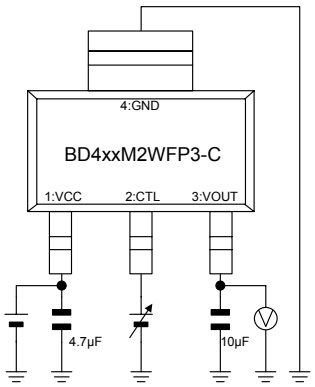
Measurement Setup for
Figure 11, 29



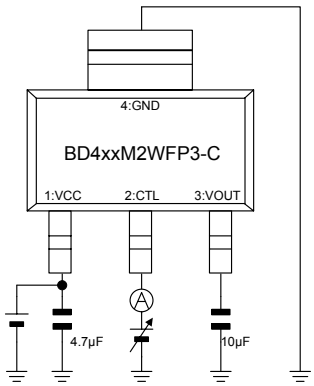
Measurement Setup for
Figure 12, 30



Measurement Setup for
Figure 13, 31

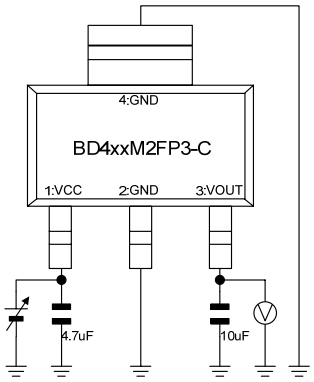


Measurement Setup for
Figure 18, 19, 20,
Figure 36, 37, 38

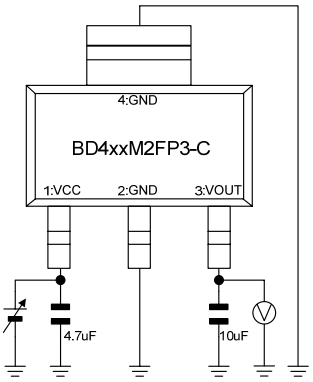


Measurement Setup for
Figure 22, 40

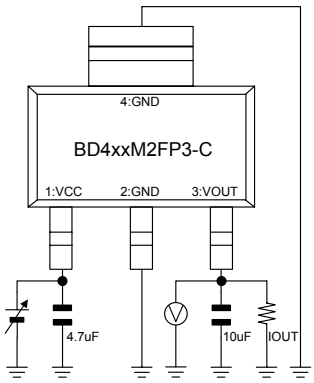
●**Measurement Circuit for Typical Performance Curves (BD433 / 450M2FP3-C)**



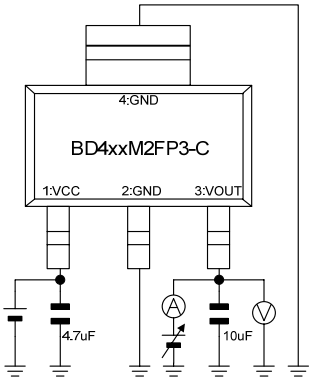
Measurement Setup for
Figure 5, 7, 16,
Figure 23, 25, 34



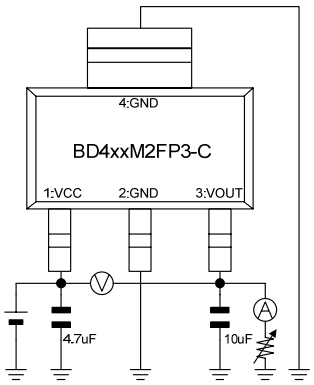
Measurement Setup for
Figure 6, 8, 14, 15,
Figure 24, 26, 32, 33



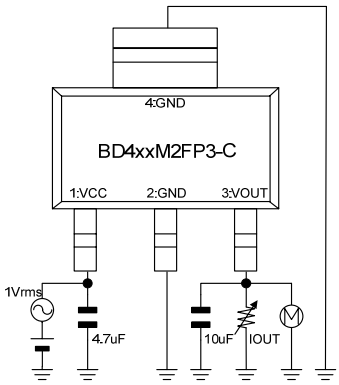
Measurement Setup for
Figure 9, 27



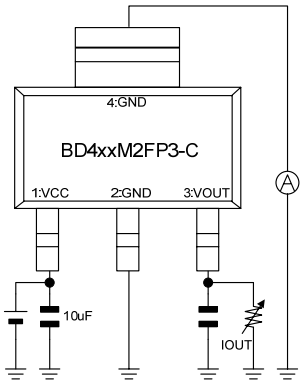
Measurement Setup for
Figure 10, 28



Measurement Setup for
Figure 11, 29



Measurement Setup for
Figure 12, 30



Measurement Setup for
Figure 13, 31

●Selection of Components Externally Connected

・VCC Pin

Insert Capacitors with a capacitance of 0.1 μF or higher between the VCC and GND pin. Choose the capacitance according to the line between the power smoothing circuit and the VCC pin. Selection of the capacitance also depends on the application. Verify the application and allow sufficient margins in the design. We recommend using a capacitor with excellent voltage and temperature characteristics.

・Output Pin Capacitor

In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. We recommend using a capacitor with a capacitance of 10 μF (Typ.) or higher. Electrolytic, tantalum and ceramic capacitors can be used. When selecting the capacitor ensure that the capacitance of 6 μF or higher is maintained at the intended applied voltage and temperature range. Due to changes in temperature the capacitor's capacitance can fluctuate possibly resulting in oscillation. For selection of the capacitor refer to the data of Figure 41.

The stable operation range given in the data of Figure 41 is based on the standalone IC and resistive load. For actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed.

When selecting a ceramic type capacitor, we recommend using X5R, X7R or better with excellent temperature and DC-biasing characteristics and high voltage tolerance.

Also, in case of rapidly changing input voltage and load current, select the capacitance in accordance with verifying that the actual application meets with the required specification.

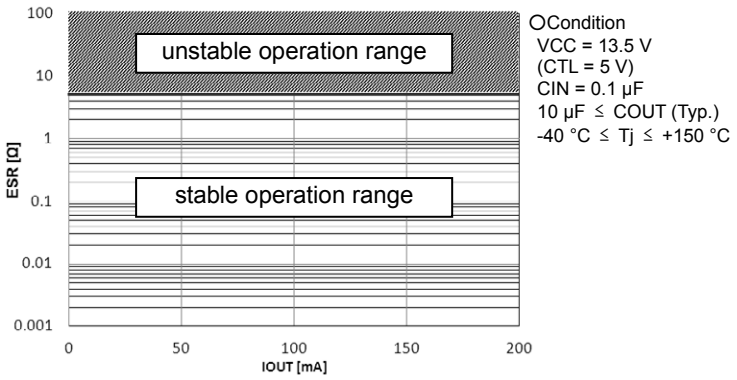


Figure 41. ESR vs. IOUT

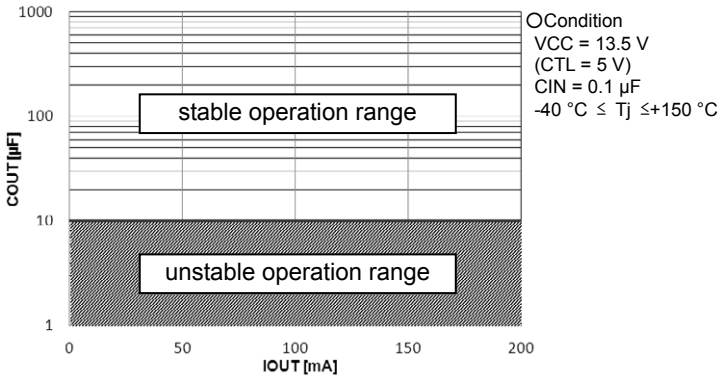


Figure 42. COUT vs. IOUT

●Measurement Setup

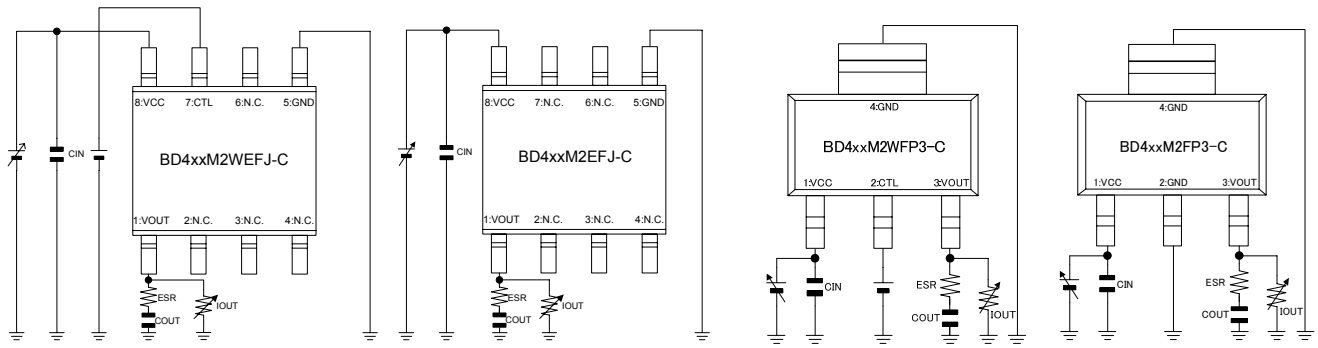
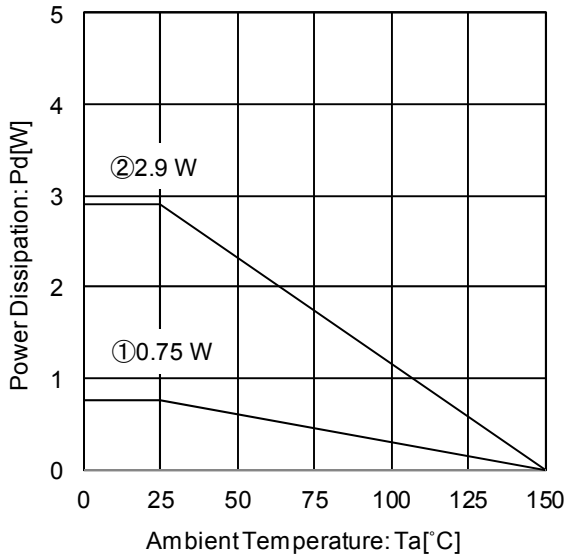


Figure 43.Measurement Setups for ESR Reference Data
(about Output Pin Capacitor)

●**Power Dissipation**

■HTSOP-J8



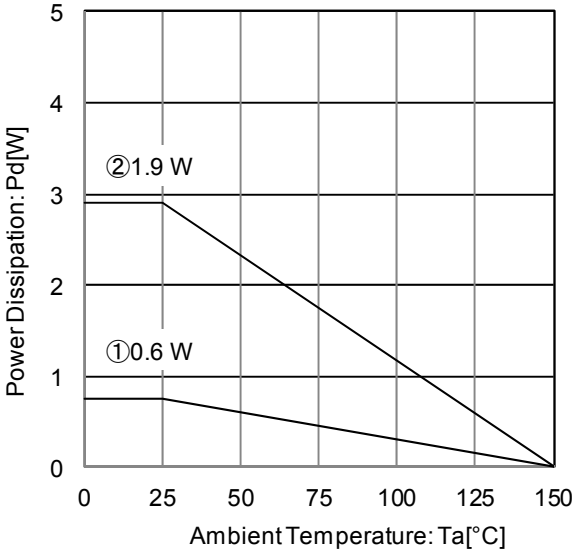
IC mounted on ROHM standard board based on JEDEC.
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.6 mmt
(with thermal via on the board)
Mount condition: PCB and exposed pad are soldered.
Top copper foil: The footprint ROHM recommend.
+ wiring to measure.

① : 1-layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
② : 4-layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB:
74.2mm x 74.2 mm)

Condition①: θja = 166.7 °C/W, θjc(top) = 45 °C/W
Condition②: θja = 43.1 °C/W, θjc(top) = 16 °C/W, θjc(bottom) = 10 °C/W

Figure 44. Package Data
(HTSOP-J8)

■SOT223-4F



IC mounted on ROHM standard board based on JEDEC.
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.6 mmt
(with thermal via on the board)
Mount condition: PCB and exposed pad are soldered.
Top copper foil: The footprint ROHM recommend.
+ wiring to measure.

① : 1-layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
② : 4-layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB:
74.2mm x 74.2 mm)

Condition①: θja = 208.3 °C/W, θjc(top) = 52 °C/W
Condition②: θja = 83.3 °C/W, θjc(top) = 36 °C/W, θjc(bottom) = 17 °C/W

Figure 45. Package Data
(SOT223-4F)

Refer to the heat mitigation characteristics illustrated in Figure 44, 45 when using the IC in an environment of Ta ≥ 25 °C.
The characteristics of the IC are greatly influenced by the operating temperature, and it is necessary to operate under the maximum junction temperature Tjmax.
Even if the ambient temperature Ta is at 25 °C it is possible that the junction temperature Tj reaches high temperatures.
Therefore, the IC should be operated within the power dissipation range.

The following method is used to calculate the power consumption Pc (W)

$$Pc = (VCC - VOUT) \times IOUT + VCC \times Icc$$
Power dissipation Pd ≥ Pc

VCC : Input Voltage
VOUT : Output Voltage
IOUT : Load Current
Icc : Circuit Current
Pc : Power Consumption

The load current IOUT is obtained by operating the IC within the power dissipation range.

$$IOUT \leq \frac{Pd - VCC \times Icc}{VCC - VOUT}$$ (Refer to Figure 13, 31 for the Icc.)

Thus, the maximum load current IOUTmax for the applied voltage VCC can be calculated during the thermal design process.
The following method is also used to calculate the junction temperature Tj.

$$Tj = Pc \times \theta jc + Tc$$

Ta : Ambient Temperature
Tc : Case Temperature
Tj : Junction Temperature
θjc : Thermal Resistance (Junction to Case)

●HTSOP-J8

■Calculation Example 1) with Ta = 105 °C VCC = 13.5 V, VOUT = 5.0 V

$$IOUT \leq \frac{1.06\ W - 13.5\ V \times Icc}{8.5\ V}$$
IOUT ≤ 125 mA (Icc: 45 μA)

(IC stand alone θja=43.1 °C/W → -23 mW/°C
25 °C = 2.9 W → 105 °C = 1.06 W)

At Ta = 105 °C with Figure 44 ② condition, the calculation shows that 125 mA of output current is possible at 8.5 V potential difference across input and output.

The thermal calculation shown above should be taken into consideration during the thermal design in order to keep the whole operating temperature range within the power dissipation range.
In the event of shorting (i.e. VOUT and GND pins are shorted) the power consumption Pc of the IC can be calculated as follows:

$$Pc = VCC \times (Icc + Ishort)$$ (Refer to Figure 10, 28 for the Ishort) Ishort : short current

■Calculation Example 2) with Tc(bottom) = 80 °C, VCC = 13.5 V, VOUT = 5.0 V, IOUT = 80 mA

At Tc(bottom) = 80 °C with Figure 44 ② condition, the power consumption Pc of the IC can be calculated as follows:

$$Pc = (VCC - VOUT) \times IOUT + VCC \times Icc$$
$$Pc = (13.5\ V - 5.0\ V) \times 80\ mA + 13.5\ V \times Icc$$
Pc = 0.681 W (Icc = 45 μA)

At the power consumption Pc is 0.681 W, the junction temperature Tj can be calculated as follows:

$$Tj = Pc \times \theta jc + Tc$$
$$Tj = 0.681\ W \times \theta jc + 80\ °C$$
Tj = 86.8 °C (θjc(bottom) = 10 °C/W)

The junction temperature is 86.8 °C, at above condition.
The thermal calculation shown above should be taken into consideration during the thermal design in order to keep the whole operating temperature range within Tj ≤ 150 °C.

●SOT223-4F

■Calculation Example 1) with Ta = 105 °C VCC = 13.5 V, VOUT = 5.0 V

$$IOUT \leq \frac{0.54\ W - 13.5\ V \times Icc}{8.5\ V}$$

$$IOUT \leq 63\ mA \quad (\ Icc: 45\ \mu A\ )$$

(IC stand alone θja = 83.3 °C/W → -12 mW/°C
25 °C = 1.50 W → 105 °C = 0.54 W)

At Ta = 105°C with Figure 45 ② condition, the calculation shows that 63 mA of output current is possible at 8.5 V potential difference across input and output.

The thermal calculation shown above should be taken into consideration during the thermal design in order to keep the whole operating temperature range within the power dissipation range.
In the event of shorting (i.e. VOUT and GND pins are shorted) the power consumption Pc of the IC can be calculated as follows:

Pc = VCC x (Icc + Ishort) (Refer to Figure 10, 28 for the Ishort)

■Calculation Example 2) with Tc(bottom) = 92 °C, VCC = 13.5 V, VOUT = 5.0 V, IOUT = 80 mA

At Tc(bottom) = 92 °C with Figure 45 ② condition, the power consumption Pc of the IC can be calculated as follows:

Pc = (VCC - VOUT) x IOUT + VCC x Icc
Pc = (13.5 V - 5.0 V) x 80 mA + 13.5 V x Icc
Pc = 0.681 W (Icc = 45 μA)

At the power consumption Pc is 0.681 W, the junction temperature Tj can be calculated as follows:

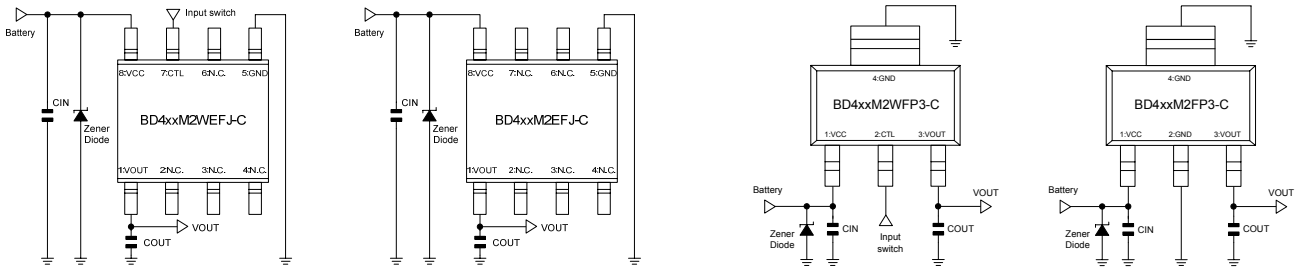
Tj = Pc x θjc + Tc
Tj = 0.681 W x θjc + 92 °C
Tj = 103.6 °C (θjc(bottom) = 17 °C/W)

The junction temperature is 103.6 °C, at above condition.
The thermal calculation shown above should be taken into consideration during the thermal design in order to keep the whole operating temperature range within Tj ≤ 150 °C.

●Application Examples

・Applying positive surge to the VCC pin

If the possibility exists that surges higher than 45 V will be applied to the VCC pin, a Zener Diode should be placed between the VCC pin and GND pin as shown in the figure below.



HTSOP-J8 SOT223-4F

Figure 48. Sample Application Circuit 1

・Applying negative surge to the VCC pin

If the possibility exists that negative surges lower than the GND are applied to the VCC pin, a Shottky Diode should be place between the VCC pin and GND pin as shown in the figure below.

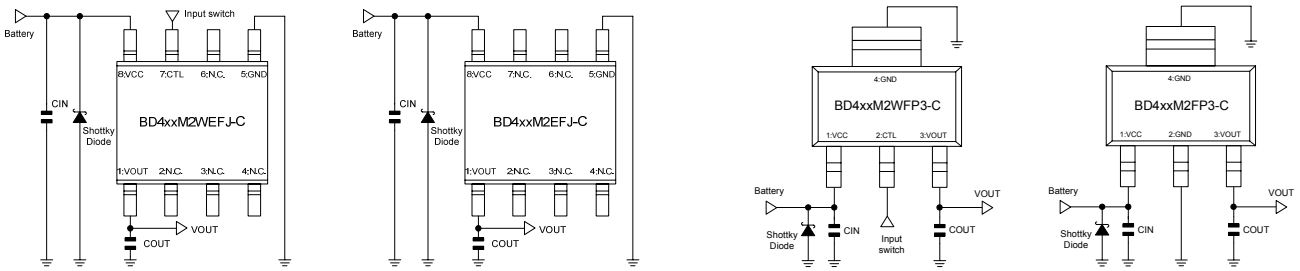


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Figure 49. Sample Application Circuit 2

・Implementing a Protection Diode

If the possibility exists that a large inductive load is connected to the output pin resulting in back-EMF at time of startup and shutdown, a protection diode should be placed as shown in the figure below.

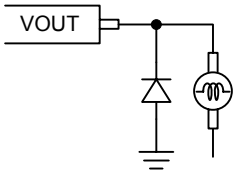


Figure 50. Sample Application Circuit 3

●I / O Equivalence Circuit

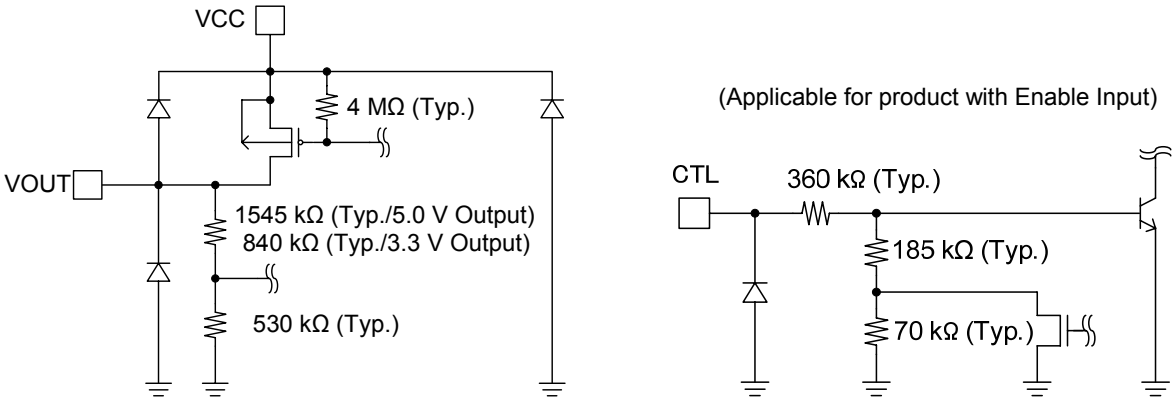


Figure 51. Input / Output Equivalence Circuit

●Operational Notes

1) Absolute Maximum Ratings
Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters can result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

2) The electrical characteristics given in this specification may be influenced by conditions such as temperature, supply voltage and external components. Transient characteristics should be sufficiently verified.

3) GND Electric Potential
Keep the GND pin potential at the lowest (minimum) level under any operating condition. Furthermore, ensure that, including the transient, none of the pin's voltages are less than the GND pin voltage.

4) GND Wiring Pattern
When both a small-signal GND and a high current GND are present, single-point grounding (at the set standard point) is recommended. This in order to separate the small-signal and high current patterns and to ensure that voltage changes stemming from the wiring resistance and high current do not cause any voltage change in the small-signal GND. Similarly, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

5) Inter-Pin Shorting and Mounting Errors
Ensure that when mounting the IC on the PCB the direction and position are correct. Incorrect mounting may result in damaging the IC. Also, shorts caused by dust entering between the output, input and GND pin may result in damaging the IC.

6) Inspection Using the Set Board
The IC needs to be discharged after each inspection process as, while using the set board for inspection, connecting a capacitor to a low-impedance pin may cause stress to the IC. As a protection from static electricity, ensure that the assembly setup is grounded and take sufficient caution with transportation and storage. Also, make sure to turn off the power supply when connecting and disconnecting the inspection equipment.

7) Power Dissipation (Pd)
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 114.3mm x 76.2mm x 1.6mmt glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

8) Thermal Design
The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed for in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. Use both the front and reverse side of the PCB to increase the heat dissipation pattern as far as possible. The amount of heat generated depends on the voltage difference across the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating.

(Tjmax: maximum junction temperature = 150°C, Ta: Ambient Temperature (°C), θja: Junction-to-Ambient Thermal Resistance (°C/W), Pd: Power Dissipation Rating (W), Pc: Power Consumption (W), VCC: Supply Voltage, VOUT: Output Voltage, IOUT: Output Current, Icc: Circuit Current)

Power Dissipation Rating	Pd (W) = (Tjmax - Ta) / θja
Power Consumption	Pc (W) = (VCC - VOUT) x IOUT + VCC x Icc

9) Overcurrent Protection Circuit
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

10) Thermal Shut Down (TSD)
This IC incorporates and integrated thermal shutdown circuit to prevent heat damage to the IC. Normal operation should be within the power dissipation rating, if however the rating is exceeded for a continued period, the junction temperature (Tj) will rise and the TSD circuit will be activated and turn all output pins OFF. After the Tj falls below the TSD threshold the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

11) In some applications, the VCC and pin potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, while the external capacitor is charged, the VCC shorts to the GND. Use a capacitor with a capacitance with less than 1000 μF. We also recommend using reverse polarity diodes in series or a bypass between all pins and the VCC pin.

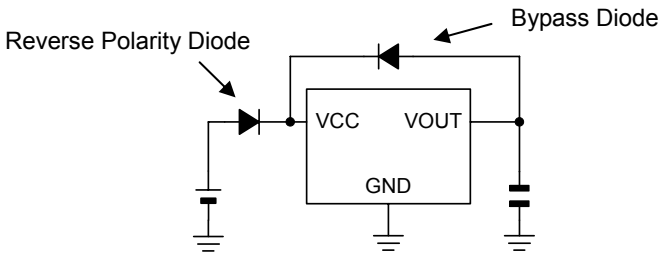


Figure 52.

12) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, in case a resistor and a transistor are connected to the pins as shown in the figure below then:
○The P/N junction functions as a parasitic diode when GND > pin A for the resistor, or GND > pin B for the transistor.
○Also, when GND > pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of the other adjacent elements to operate as a parasitic NPN transistor.
Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits and can cause malfunctions and, in turn, physical damage to or destruction of the chip. Therefore do not employ any method in which parasitic diodes can operate such as applying a voltage to an input pin that is lower than the (P substrate) GND.

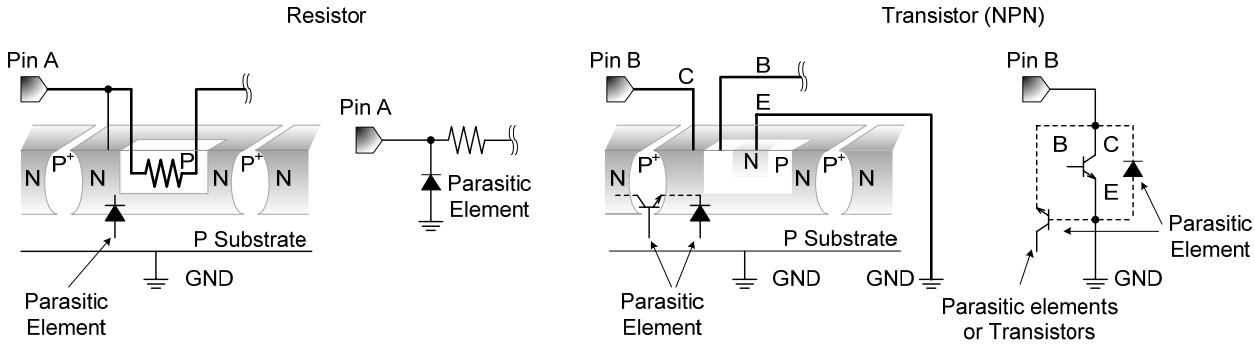
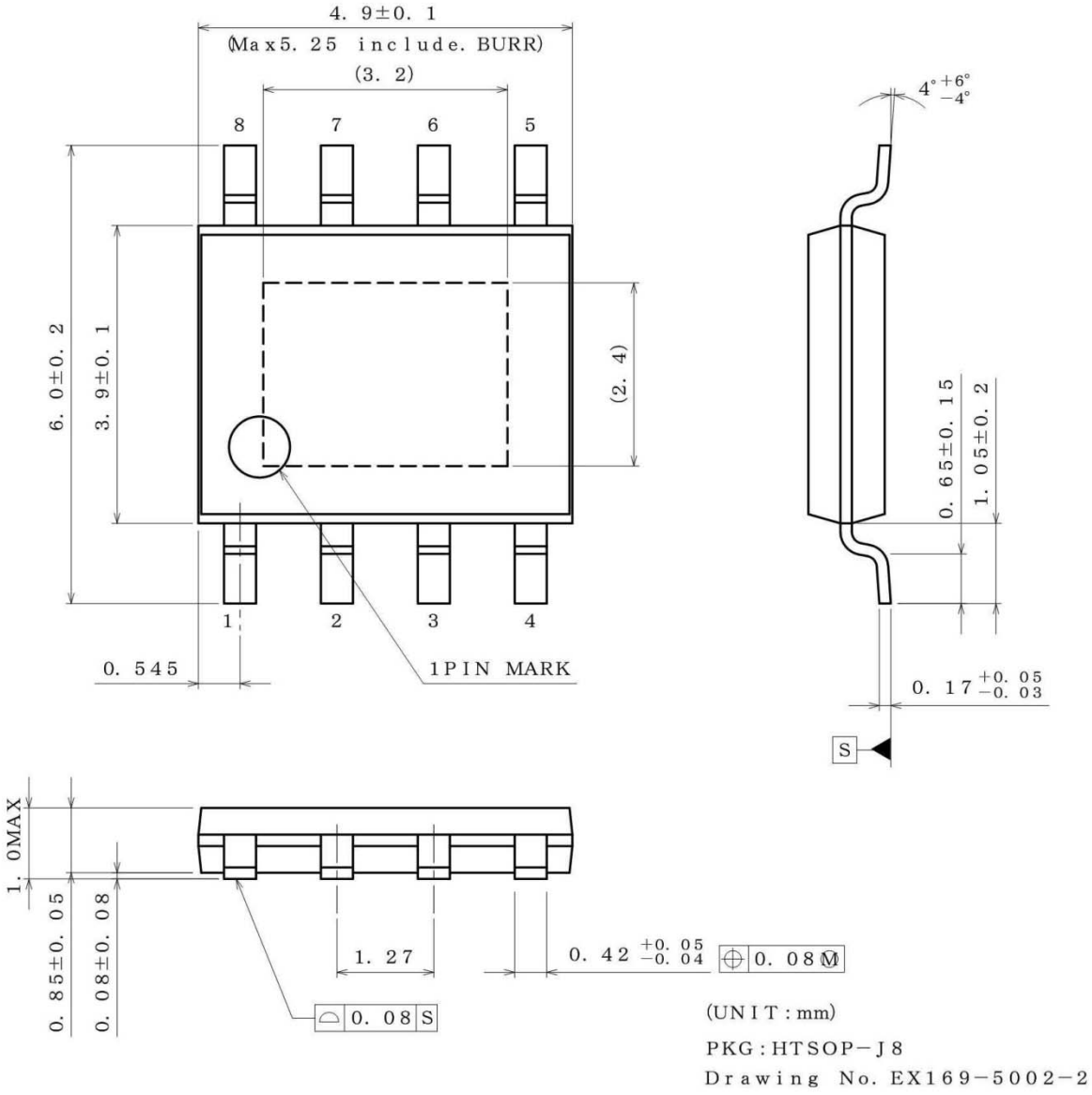


Figure 53.

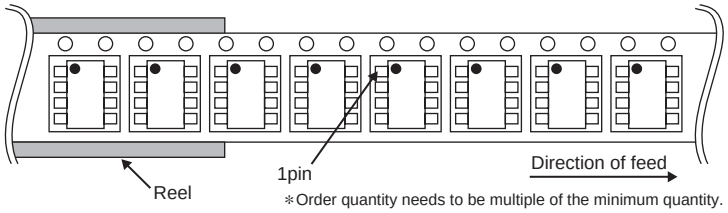
●**Physical Dimension, Tape and Reel Information (HTSOP-J8)**

Package Name	HTSOP-J8



<Tape and Reel information>

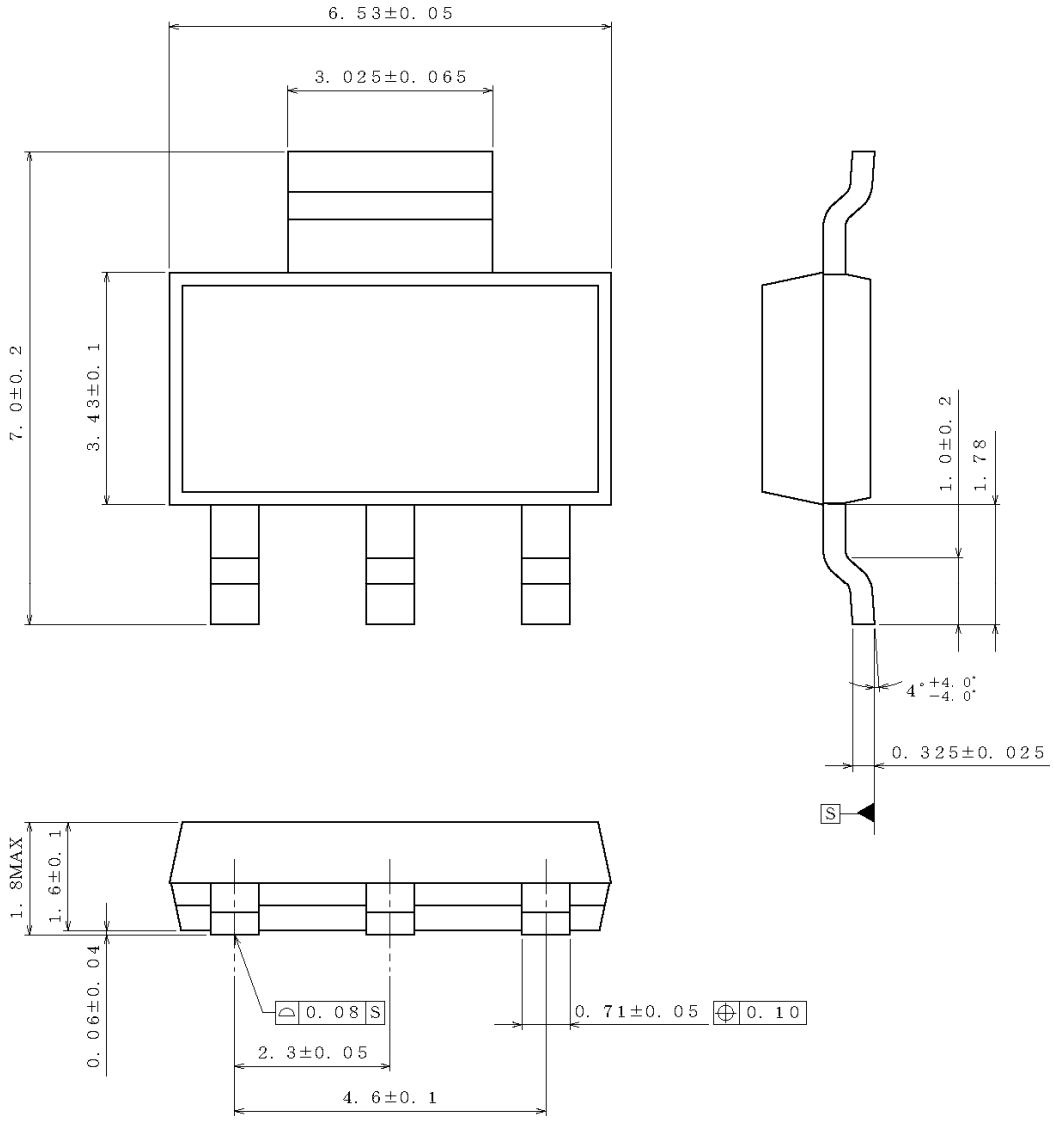
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●**Physical Dimension, Tape and Reel Information (SOT223-4F)**

Package Name	SOT223-4F

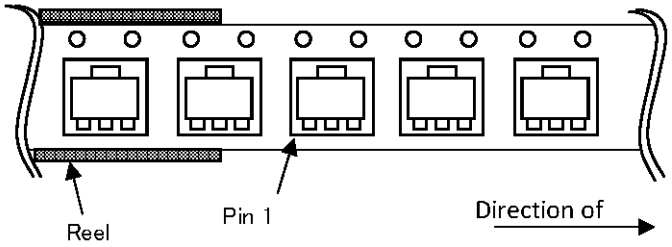


(UNIT mm)

Drawing No. EX561-5001

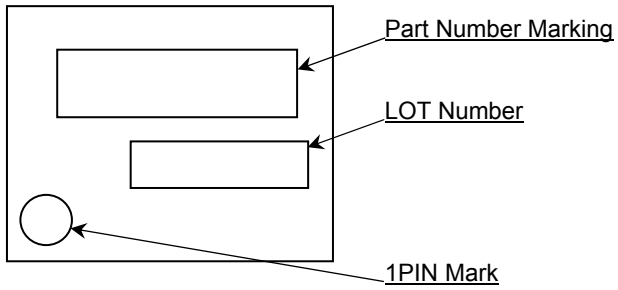
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand)



●**Marking Diagrams (Top View)**

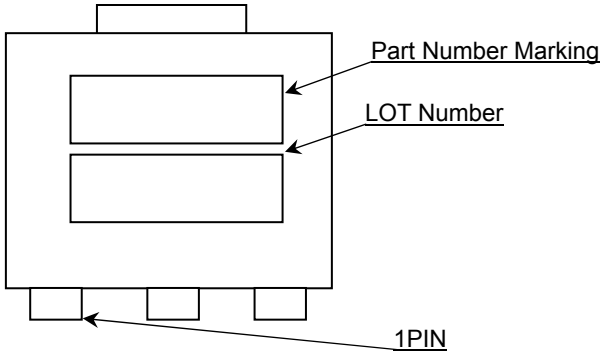
HTSOP-J8 (Top View)



Part Number Marking	Output Voltage [V]	Enable Input *1
433M2W	3.3	○
450M2W	5.0	○
433M2	3.3	－
450M2	5.0	－

*1 ○: Includes Enable Input
－: Not includes Enable Input

SOT223-4F (Top View)



Part Number Marking	Output Voltage [V]	Enable Input *1
433M2W	3.3	○
450M2W	5.0	○
433M2	3.3	－
450M2	5.0	－

*1 ○: Includes Enable Input
－: Not includes Enable Input

●**Revision History**

Date	Revision	Changes
05.Dec.2012	001	New Release (BD450M2WEFJ-C, BD450M2EFJ-C)
15.Jan.2013	002	Additional Entry (BD4xxM2-C Series)